1. Introduction

This application note provides an interesting descriptive and practical introduction to the golden rules to be followed in the successful use of SCRs and triacs in power control applications

2. SCR

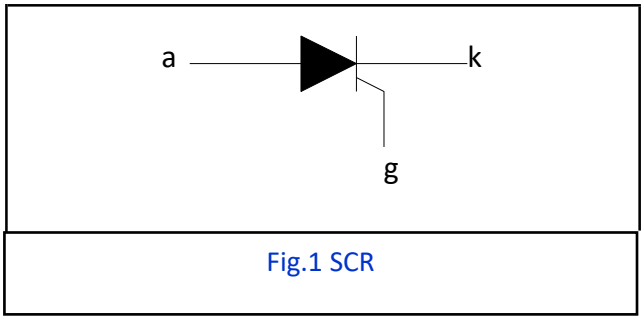

Fig.1 SCR

An SCR is a silicon-controlled rectifier (Fig. 1) where the unidirectional current flow from anode to cathode is initiated by a small signal current from gate to cathode. The SCR's operating characteristic is shown below in Fig. 2

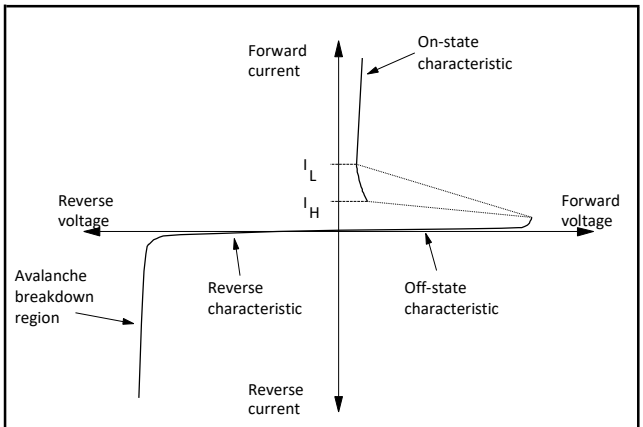

Fig. 2. Thyristor V/I characteristic

2.1 SCR Turn-on

An SCR is turned-on by making its gate positive with respect to its cathode, thereby causing current flow into the gate. When the gate voltage reaches the threshold voltage V_{GT} and the resulting current reaches the threshold current I_{GT}, within a very short time known as the gate-controlled turn-on time, t_{gt}, the load current can flow from 'a' to 'k'. If the gate current consists of a very narrow pulse, say less than 1µs, its peak level will have to increase for progressively narrower pulse widths to guarantee triggering.

When the load current reaches the thyristor's latching current I_L, load current flow will be maintained even after removal of the gate current. If adequate load current continues to flow, the thyristor will continue to conduct without the gate current. It is said to be latched ON.

Note that the V_{GT}, I_{GT} and I_L specifications given in data are at 25 ˚C. These parameters will increase at lower temperatures, so the drive circuit must provide adequate voltage and current amplitude and duration for the lowest expected operating temperature.

> *Rule 1. To turn a SCR (or triac) ON, a gate current ≥ I_{GT} must be applied until the load current is ≥ I_L. This condition must be met at the lowest expected operating temperature.*

Sensitive gate thyristors such as the BT150 can be prone to turn-on by anode to cathode leakage current at high temperatures. If the junction temperature T_j is increased above T_j max, a point will be reached where the leakage current will be high enough to trigger the thyristor's sensitive gate. It will then have lost its ability to remain in the blocking state and conduction will commence without the application of an external gate current.

1. Ensure that the temperature does not exceed T_j max.

2. Use an SCR with a less sensitive gate such as the BT151 or reduce the existing SCR's sensitivity by including a gate-to-cathode resistor of 1kΩ or less.

3. If it is not possible to use a less sensitive thyristor due to circuit requirements, apply a small degree of reverse biasing to the gate during the 'off' periods. This has the effect of increasing I_L. During negative gate current flow, attention should be paid to minimising the gate power dissipation.

2.2 SCR Turn-off (commutation)

In order to turn the SCR off, the load current must be reduced below its holding current I_H for sufficient time to allow all the mobile charge carriers to vacate the junction. This is achieved by "forced commutation" in DC circuits or at the end of the conducting half cycle in AC circuits. (Forced commutation is when the load circuit causes the load current to reduce to zero to allow the SCR to turn off.) At this point, the SCR will have returned to its fully blocking state.

If the load current is not maintained below I_H for long enough, the SCR will not have returned to the fully blocking state by the time the anode-to-cathode voltage rises again. It might then return to the conducting state without an externally-applied gate current.

Note that I_H is also specified at room temperature and, like I_L, it reduces at higher temperatures. The circuit must therefore allow sufficient time for the load current to fall below I_H at the maximum expected operating temperature for successful commutation.

Rule 2. To turn off (commutate) an SCR (or triac), the load current must be < I_H for sufficient time to allow a return to the blocking state. This condition must be met at the highest expected operating temperature.

3. Triac

A triac can be regarded as a "bidirectional thyristor" because it conducts in both directions. For standard triacs, current flow in either direction between the main terminals MT1 and MT2 is initiated by a small signal current applied between MT1 and the gate terminal.

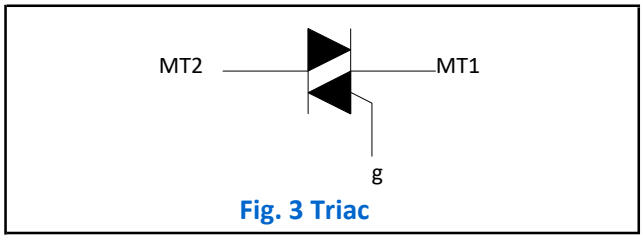

Fig. 3 Triac

3.1 Triac Turn-on

Unlike thyristors, standard triacs can be triggered by positive or negative current flow between the gate and MT1. (The rules for V_{GT}, I_{GT} and I_L are the same as for thyristors. See Rule 1.) This means there can be triggering in four "quadrants" as summarised below.

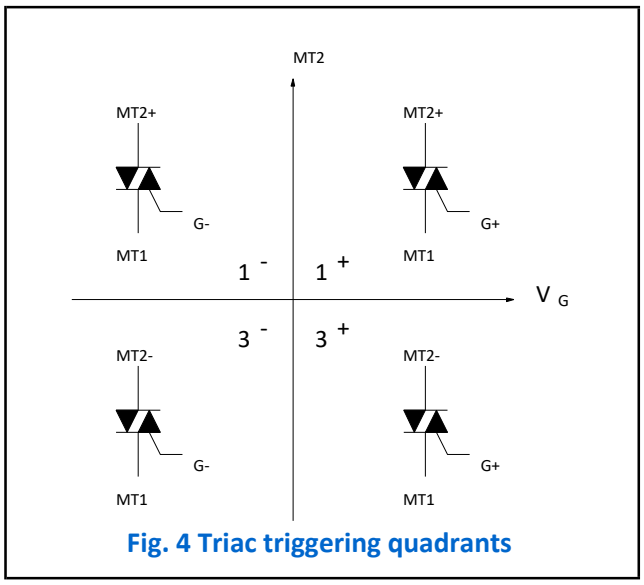

Fig. 4 Triac triggering quadrants

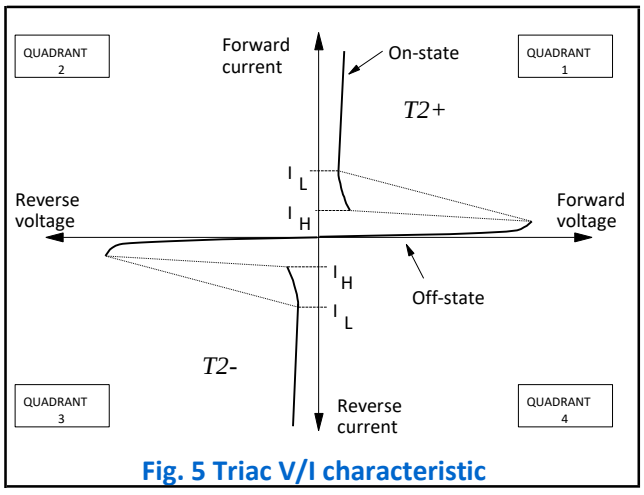

Fig. 5 Triac V/I characteristic

Where the gate is to be triggered by DC or unipolar pulses at zero-crossing of the load current, negative gate current is to be preferred. The internal construction of the triac means that the gate is more remote from the main current-carrying region when operating in the 3^+ quadrant. This results in: -

1. Higher I_{GT} -> higher peak I_G required.

2. Longer delay between I_G and the commencement of load current flow -> longer duration of I_G required.

3. Much lower dI_T/dt capability -> progressive gate degradation can occur when controlling loads with high initial dI/dt (e.g. cold incandescent lamp filaments).

4. Higher I_L (also true for 1^- operation) -> longer I_G duration may be needed for very small loads when conducting from the beginning of a mains half cycle to allow the load current to reach the higher I_L.

In standard AC phase control circuits such as lamp dimmers and domestic motor speed controls, the gate and MT2 polarities are always the same. This means thatoperationisalwaysinthe1^+ and3^- quadrants where the triac's switching parameters are the same. This results in symmetrical triac switching where the gate is at its most sensitive.

Note that the 1^+, 1^-, 3^- and 3^+ notation for the four triggering quadrants is used for brevity instead of writing "MT2+, G+" for 1^+, etc. This notation is derived from the graph of the triac's V/I characteristic. Positive MT2 corresponds with positive current flow into MT2, and vice versa (see Fig. 5). Hence, operation is in quadrants 1 and 3 only. The + and - superscripts refer to inward and outward gate current respectively.

> *Rule 3. When designing a triac triggering circuit, avoid triggering in the 3+ quadrant (MT2, G+) where possible*

3.2 Alternative triac turn-on methods

There are undesirable ways a triac can be turned on. Some are benign, while some are potentially destructive.

3.2.1 Noisy gate signal

In electrically noisy environments, spurious triggering can occur if the noise voltage on the gate exceeds V_{GT} and enough gate current flows to initiate regenerative action within the triac. The first line of defence is to minimise the occurrence of the noise in the first place. This is best achieved by keeping the gate connections as short as possible and ensuring that the common return from the gate drive circuit connects directly to the MT1 pin (or cathode in the case of an SCR). In situations where the gate connections are hard wired, twisted pair wires or even shielded cable might be necessary to minimise pickup.

Additional noise immunity can be provided by adding a resistor of 1kΩ or less between the gate and MT1 to reduce the gate sensitivity. If a high frequency bypass capacitor is also used, it is advisable to include a

series resistor between it and the gate to minimise peak capacitor currents through the gate and minimise the possibility of overcurrent damage to the triac's gate area. **Alternatively, use a series H triac (e.g. BT139-600H). These are insensitive types with 10mA min I_{GT} specs which are specifically designed to provide a high degree of noise immunity.**

> *Rule 4. To minimize noise pick-up, keep gate connection length to a minimum. Take the return directly to MT1 (or cathode). If hard wired, use twisted pair or shielded cable. Fit a resistor of 1kΩ or less between gate and MT1. Fit a bypass capacitor in conjunction with a series resistor to the gate. Alternatively, use an in sensitive series H triac.*

3.2.2 Exceeding the maximum rate of change of commutating voltage dV_{com}/dt

This is most likely to occur when driving a highly reactive load where there is substantial phase shift between the load voltage and current waveforms. When the triac commutates as the load current passes through zero, the voltage will not be zero because of the phase shift (see Fig. 6). The triac is then suddenly required to block this voltage. The resulting rate of change of commutating voltage can force the triac back into conduction if it exceeds the permitted dV_{COM}/dt. This is because the mobile charge carriers have not been given time to clear the junction.

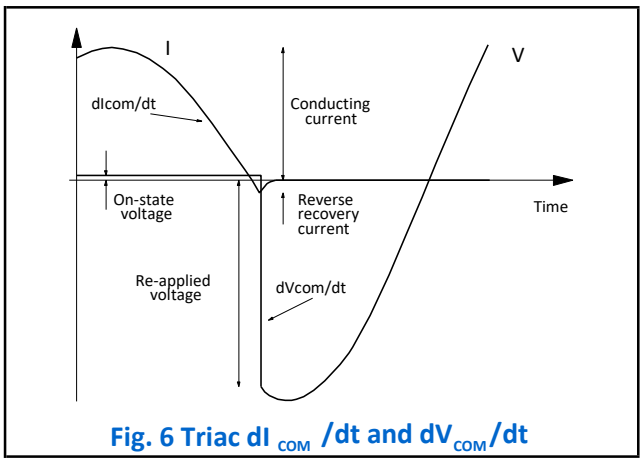

Fig. 6 Triac dI_{COM}/dt and dV_{COM}/dt

The dV_{COM}/dt capability is affected by two conditions: -

1. The rate of fall of load current at commutation, dI_{COM}/dt. Higher dI_{COM}/dt lowers the dV_{COM}/dt capability.

2. The junction temperature T_j. Higher T_j lowers the dV_{COM}/dt capability.

If the triac's dV_{COM}/dt is likely to be exceeded, false triggering can be avoided by use of an RC snubber across MT1-MT2 to limit the rate of change of voltage. Common values are 100Ω carbon composition resistor, chosen for its surge current handling, and 100nF.

Alternatively, use a Hi-Com triac.

Note that the resistor should never be omitted from the snubber because there would then be nothing to prevent the capacitor from dumping its charge into the triac and creating damaging dI_T/dt during unfavourable turn-on conditions.

3.2.3 Exceeding the maximum rate of change of commutating current dI_{com}/dt

Higher dI_{COM}/dt is caused by higher load current, higher mains frequency (assuming sinewave current) or non-sinewave load current. A well-known cause of non-sinewave load current and high dI_{COM}/dt is rectifier-fed inductive loads. These can often result in commutation failure in standard triacs as the supply voltage falls below the back EMF of the load and the triac current collapses suddenly to zero. The effect of this is illustrated in Fig. 7.

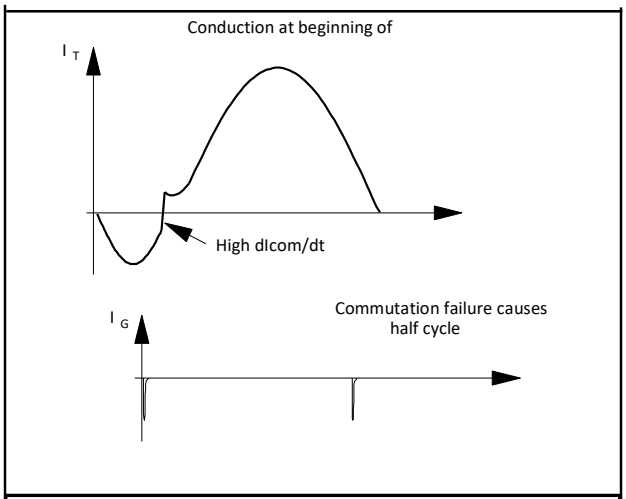

Fig. 7. Effects of rectifier-fed inductive load on phase control circuit

3.2.4 Exceeding the maximum rate of change of on-state voltage dV_D/dt

If a very high rate of change of voltage is applied across a non-conducting triac (or sensitive gate SCR in particular) without exceeding its V_{DRM} (see Fig. 8), internal capacitive current can generate enough gate current to trigger the device into conduction.

Susceptibility is increased at high temperature.

Where this is a problem, the dV_D/dt must be limited by an RC snubber across MT1 and MT2 (or anode and cathode). **In the case of triacs, using Hi-Com types can yield benefits.**

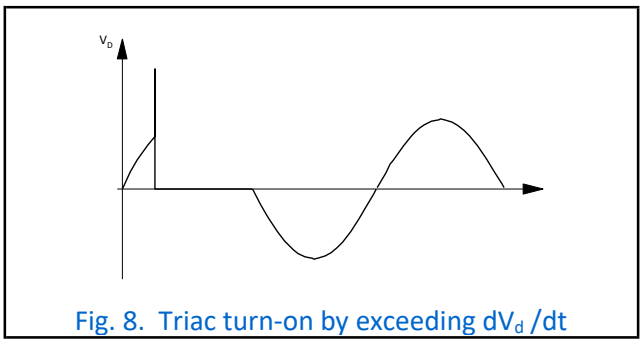

Fig. 8. Triac turn-on by exceeding dV_d/dt

Rule 5. Where high dV_D/dt or dV_{COM}/dt are likely to cause a problem, fit an RC snubber across MT1 and MT2. Where high dI_{COM}/dt is likely to cause a problem, fit an inductor of a few mH in series with the load. Alternatively, use a Hi-Com triac.

3.2.5 Exceeding the repetitive peak off-state voltage V_{DRM}

If the MT2 voltage exceeds V_{DRM} such as might occur during severe and abnormal mains transient conditions, MT2-MT1 leakage will reach a point where the triac will spontaneously break over into conduction (see Fig. 9).

If the load permits high inrush currents to flow, extremely high localised current density can occur in the small area of silicon that is conducting. This can lead to burnout and destruction of the die. Incandescent lamps, capacitive loads and crowbar protection circuits are the likely causes of high inrush currents.

Turn-on by exceeding the triac's V_{DRM} or dV_D/dt is not necessarily the main threat to its survival. It's the dI_T/dt that follows which is most likely to cause the damage. Due to the time required for conduction to spread out over the whole junction, the permitted dI_T/dt is lower than if the triac is correctly turned on by a gate signal. If the dI_T/dt can be limited during these conditions to this lower value, which is given in

data, the triac is more likely to survive. This could be achieved by fitting a non-saturable (air cored) inductor of a few µH in series with the load.

If the above solution is unacceptable or impractical, an alternative solution would be to provide additional filtering and clamping to prevent the spikes reaching the triac. This would probably involve the use of a Metal Oxide Varistor as a "soft" voltage clamp across the supply, with series inductance followed by parallel capacitance upstream of the MOV.

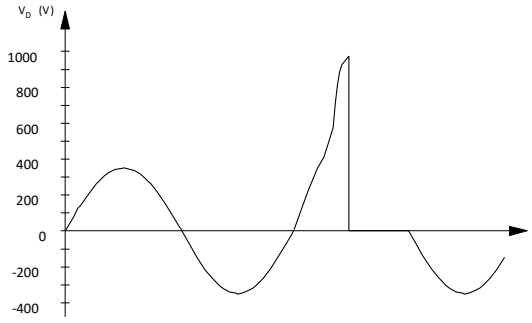

Fig. 9 Triac turn-on by exceeding V_{DRM}

Doubts have been expressed by some manufacturers over the reliability of circuits which use MOVs across the mains, since they have been known to go into thermal runaway in high ambient temperatures and fail catastrophically. This is due to the fact that their operating voltage possesses a marked negative temperature coefficient. However, if the recommended voltage grade of 275V RMS is used for 230V mains, the risk of MOV failure should be negligible. Such failures are more likely if 250V RMS MOVs are used, which are underspecified for 230V RMS use at high ambient temperatures.

Rule 6. If the triac's V_{DRM} is likely to be exceeded during severe mains transients, employ one of the following measures: limit high dI_T/dt with a non-saturable inductor of a few µH in series with the load or use a MOV across the mains in combination with filtering on the supply side.

3.2.6 Turn-on dI_T/dt

When a triac or thyristor is triggered into conduction by the correct method via its gate, conduction begins in the die area immediately adjacent to the gate, then quickly spreads to cover the whole active area. This time delay imposes a limit on the permissible rate of rise of load current. A dI_T/dt which is too high can cause localised burnout. An MT1-MT2 short will be the result.

If triggering in the 3^+ quadrant, an additional mechanism further reduces the permitted dI_T/dt. It is possible to momentarily take the gate into reverse avalanche breakdown during the initial rapid current rise. This might not lead to immediate failure. Instead, there would be progressiveburnoutofthegate-MT1shortingresistance after repeated exposure. This would show itself by a progressive increase in I_{GT} until the triac will no longer trigger. Sensitive triacs are likely to be the most susceptible. Hi-Com triacs are not affected as they do not operate in the 3+ quadrant.

The dI_T/dt capability is affected by how fast the gate current rises (dI_G/dt) and the peak value of I_G. Higher values of dI_G/dt and peak I_G (without exceeding the gate power ratings) give a higher dI_T/dt capability.

> *Rule 7. Healthy gate drive and avoiding 3^+ operation maximises the triac's dI_T/dt capability.*

As mentioned previously, a common load with a high initial surge current is the incandescent lamp which has a low cold resistance. For resistive loads such as this, the dI_T/dt would be at its highest if conduction commenced at a peak of the mains voltage. If this is likely to exceed the triac's dI_T/dt rating, it should be limited by the inclusion of an inductor of a few µH or even a Negative Temperature Coefficient thermistor in series with the load. Again, the inductor must not saturate during the maximum current peak. If it does, its inductance would collapse, and it would no longer limit the dI_T/dt. An air cored inductor meets the requirement.

A more elegant solution which could avoid the requirement for a series current-limiting device would be to use zero voltage turn-on. This would allow the current to build up more gradually from the beginning of the sinewave.

Note: It is important to remember that zero voltage turn-on is only applicable to resistive loads. Using the same method for reactive loads where there is phase shift between voltage and current can cause "half waving" or unipolar conduction, leading to possible saturation of inductive loads, damagingly high peak currents and overheating. More advanced control employing zero current switching and/or variable trigger angle is required in this case.

> *Rule 8. If the triac's dI_T/dt is likely to be exceeded, an air cored inductor of a few µH or an NTC thermistor should be fitted in series with the load. Alternatively, employ zero voltage turn-on for resistive loads.*

3.3 Triac Turn-off

Unlike thyristors, standard triacs can be triggered by positive or negative current flow between the gate and MT1. (The rules for V_{GT}, I_{GT} and I_L are the same as for thyristors. See Rule 1.) This means there can be triggering in four "quadrants" as summarised below.

3.4 Hi-Com triac

Hi-Com triacs have a different internal construction to conventional triacs. One of the differences is that the two "thyristor halves" are better separated to reduce the influence that they have on each other. This has yielded two benefits:

1.Higher dV_{COM}/dt.

This enables them to control reactive loads without the need for a snubber in most cases while still avoiding commutation failure. This reduces the component count, board size and cost, and eliminates snubber power dissipation.

2. Higher dI_{COM}/dt.

This drastically improves the chances of successfully commutating higher frequency or non-sine wave currents without the need for a dI_{COM}/dt-limiting inductor in series with the load.

3. Higher dV_D/dt.

Triacs become more sensitive at high operating temperatures. The higher dV_D/dt of Hi-Com triacs reduces their tendency to spurious dV/dt turn-on when in the blocking state at high temperature. This enables them to be used in high temperature applications controlling resistive loads, such as cooking or heating applications, where conventional triacs could not be used.

The different internal construction also means that 3^+ triggering is not possible. This should not be a problem in most cases because this is the least desirable and least used triggering quadrant, so direct substitution of a Hi-Com for an equivalent conventional triac will almost always be possible.

4. Mounting methods

For small loads or very short duration load current (i.e. less than 1 second), it might be possible to operate the triac in free air. In most cases, however, it would be fixed to a heatsink or heat dissipating bracket.

The three main methods of clamping the triac or SCR to a heat sink are clip mounting, screw mounting and riveting. Mounting kits are available from many sources for the first two methods. Riveting is not a recommended method in most cases.

4.1 Clip mounting

This is the preferred method for minimum thermal resistance. The clip exerts pressure on the plastic body of the device. It is equally suitable for the non-isolated packages (SOT82 and TO220) and the isolated package (TO220F).

4.2 Screw mounting

1. An M3 screw mounting kit for the SOT78 package includes a rectangular washer which should be between the screw head and the tab. It should not exert any force on the plastic body of the device.

2. During mounting, the screwdriver blade should never exert force on the plastic body of the device.

3. The heatsink surface in contact with the tab should be deburred and flat to within 0.02mm in 10mm.

4. The mounting torque (with washer) should be between 0.55Nm and 0.8Nm.

5. Where an alternative exists, the use of self-tapping screws should be avoided due to the possible swelling of the heatsink material around the fixing hole. This could be detrimental to the thermal contact between device and heatsink. (See 3 above.) The uncontrollable mounting torque is also a disadvantage with this fixing method.

6. The device should be mechanically fixed before the leads are soldered. This minimises undue stress on the leads.

4.3 Riveting

Pop riveting is not recommended unless great care is taken because the potentially severe forces resulting from such an operation can deform the tab and crack the die, rendering the device useless. In order to minimise rejects, the following rules should be obeyed if pop riveting: -

1. The heatsink should present a flat, burr-free surface to the device.

2. The heatsink mounting hole diameter should be no greater than the tab mounting hole diameter.
3. The pop rivet should just be a clearance fit in the tab-hole and heatsink mounting hole without free play.
4. The pop rivet should be fitted with its head, not the mandrel, on the tab side.
5. The pop rivet should be fitted at 90 degrees to the tab. (The rivet head should be in contact with the tab around its complete circumference.)
6. The head of the rivet should not be in contact with the plastic body of the device after riveting.
7. Mechanical fixing of the device and heatsink assembly to the PCB should be completed before the leads are soldered to minimise stressing of the leads.

> *Rule 9. Avoid mechanical stress to the triac when fitting it to the heatsink. Fix, then solder. Never pop rivet with the rivet mandrel on the tab side.*

5. Thermal resistance

Thermal resistance R_{th} is the resistance to the flow of heat away from the junction. It is analogous to electrical resistance; i.e. just as electrical resistance R = V/I, thermal resistance R_{th} = T/P, where T is the temperature rise in Kelvin and P is the power dissipation in Watts. Therefore, R_{th} is expressed in K/W.

For a device mounted vertically in free air, the thermal resistance is dictated by the junction-to-ambient thermal resistance $R_{th(j-a)}$. This is typically 100K/W for theSOT82 package,60K/W for the TO220 package and 55K/W for the TO220F.

For a non-isolated device mounted to a heatsink, the junction-to-ambient thermal resistance is the sum of the junction-to-mounting base, mounting base-to-heatsink and heatsink-to-ambient thermal resistances.

$R_{th(j-a)} = R_{th(j-mb)} + R_{th(mb-h)} + R_{th(h-a)}$ (non-isolated package).

The use of heat transfer compound or sheet between the device and heatsink is always recommended. In the case of isolated packages, there is no reference made to "mounting base", since the $R_{th(mb-h)}$ is assumed to be constant and optimised with heat transfer compound. Therefore, the junction-to-ambient thermal resistance is the sum of the junction-to-heatsink and heatsink-to-ambient thermal resistances.

$R_{th(j-a)} = R_{th(j-h)} + R_{th(h-a)}$ (isolated package).

$R_{th(j-mb)}$ or $R_{th(j-h)}$ are fixed and can be found in data for each device.

$R_{th(mb-h)}$ is also given in the mounting instructions for several options of insulated and non-insulated mounting, with or without heatsink compound.

$R_{th(h-a)}$ is governed by the heatsink size and the degree of unrestricted air movement past it.

5.1 Calculation of heatsink size

To calculate the required-heatsink thermal resistance for a given triac and load current, we must first calculate the power dissipation in the triac using the following equation:

$$P = V_o \times I_{T(AVE)} + R_s \times I_{T(RMS)}^2$$

Knee voltage V_0 and slope resistance R_S are obtained from the relevant V_T graph in the data sheet.

If the values are not already provided, they can be obtained from the graph by drawing a tangent to the max V_T curve. The point on the V_T axis where the tangent crosses gives V_0, while the slope of the tangent (V_T/I_T) gives R_S.

Using the thermal resistance equation given above: -

$$R_{th(j-a)} = T/P$$

The max allowable junction temperature rise will be when T_j reaches T_j max in the highest ambient temperature. This gives us T.

$R_{th(j-a)} = R_{th(j-mb)} + R_{th(mb-h)} + R_{th(h-a)}$. The datasheet gives us the values for $R_{th(j-mb)}$ and $R_{th(mb-h)}$ for our chosen mounting method, leaving $R_{th(h-a)}$ as the only unknown.

5.2 Thermal impedance

The above calculations for thermal resistance are applicable to the steady state condition - that is for a duration greater than 1 second. This time enough for heat to flow from the junction to the heatsink. For current pulses or transients lasting for shorter than 1 second, however, heatsinking has progressively less effect. The heat is simply dissipated in the bulk of the device with very little reaching the heatsink. For transient conditions such as these, the junction temperature rise is governed by the device's junction-to-mounting base thermal impedance $Z_{th(j-mb)}$.

$Z_{th(j-mb)}$ decreases for decreasing current pulse duration due to reduced chip heating. As the duration increases towards 1 second, $Z_{th(j-mb)}$ increases to the steady state

$R_{th(j-mb)}$ value.

The $Z_{th(j-mb)}$ curve for bidirectional and unidirectional current down to 10µs duration is shown for each device in the data sheet.

Rule 10. For long term reliability, ensure that the $R_{th(j-a)}$ is low enough to keep the junction temperature within $T_{j(max)}$ for the highest expected ambient temperature.

6. Product range and packaging

WeEn SCRS range from 0.8A in TO92 (SOT54) to 25A in TO220 (SOT78) and TO220F (Sot186A) to 162A in TO247 (SOT429).

WeEn triacs range from 0.8A in SOT223 and TO92 to higher currents in TO220F, TO220 and IITO220 (SOT78D) to the highest current of 45A in IITO3P (SOT1292). Conventional types (4-quadrant triggering) and Hi-Com types (3-quadrant triggering) are available.

The surface mount SOT223 and the leaded TO92 are the smaller packages for SCRs and triacs (Fig. 10). The power dissipation is governed by the degree of heatsinking offered by the PCB onto which the package is soldered.

The same respective chips are also available in SOT82 which is a non-isolated package (Fig. 12). The improved heat removal of this package when heat sunk allows higher current ratings and improved power dissipations.

Fig. 11 shows TO92 in which small devices are mounted. Smaller chips than those accommodated by SOT223 go into this package, which offers the most compact non-surface mount solution.

TO220 is the most common non-isolated package in which most of our devices are supplied (Fig. 13).

The TO220F “full pack” package shown in Fig. 14 possesses several advantages over older types.

1. It has the same dimensions as the TO220 package for pin spacing from the mounting surface, so it can directly replace TO220 devices to provide isolation without the need for modification of the mounting arrangement.
2. It has no exposed metal at the top of the tab, and creepage distances from pins to heatsink are greater, so it can offer an improved true isolation of 2,500V RMS.
3. It is a fully encapsulated TO220 replacement.

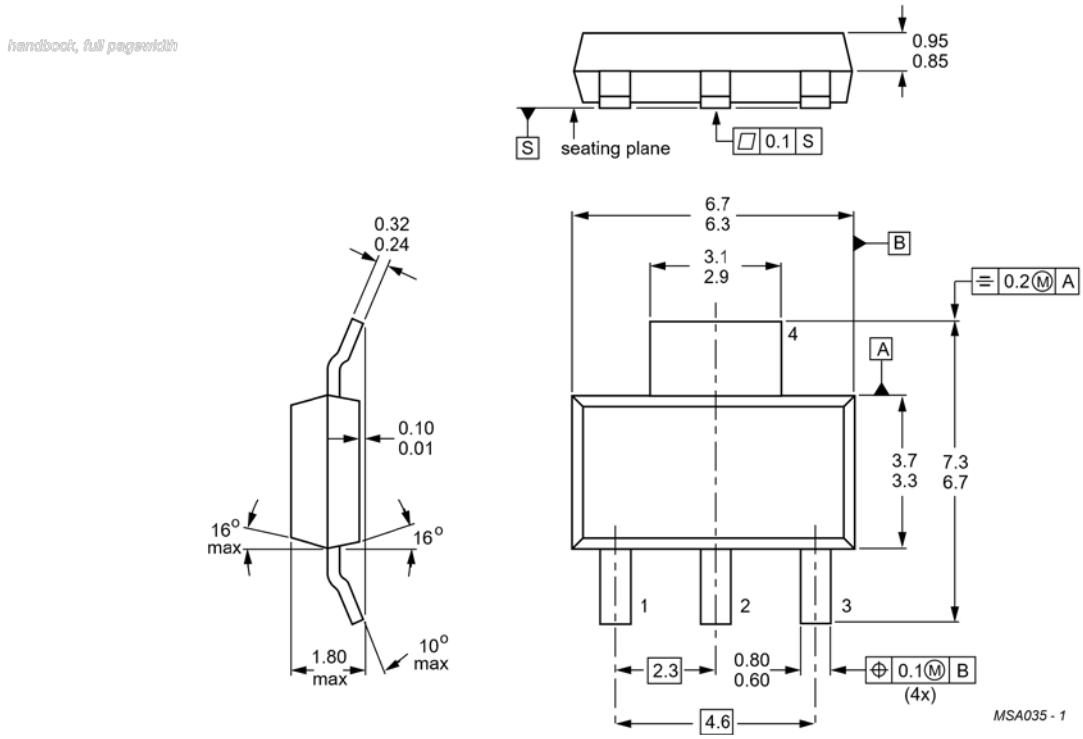

Fig. 10 SOT223

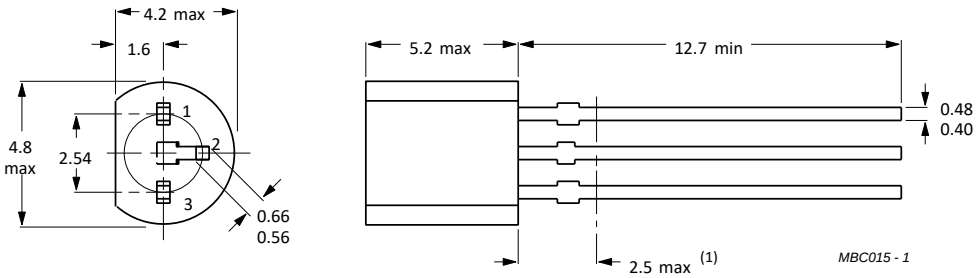

Fig 11 TO92

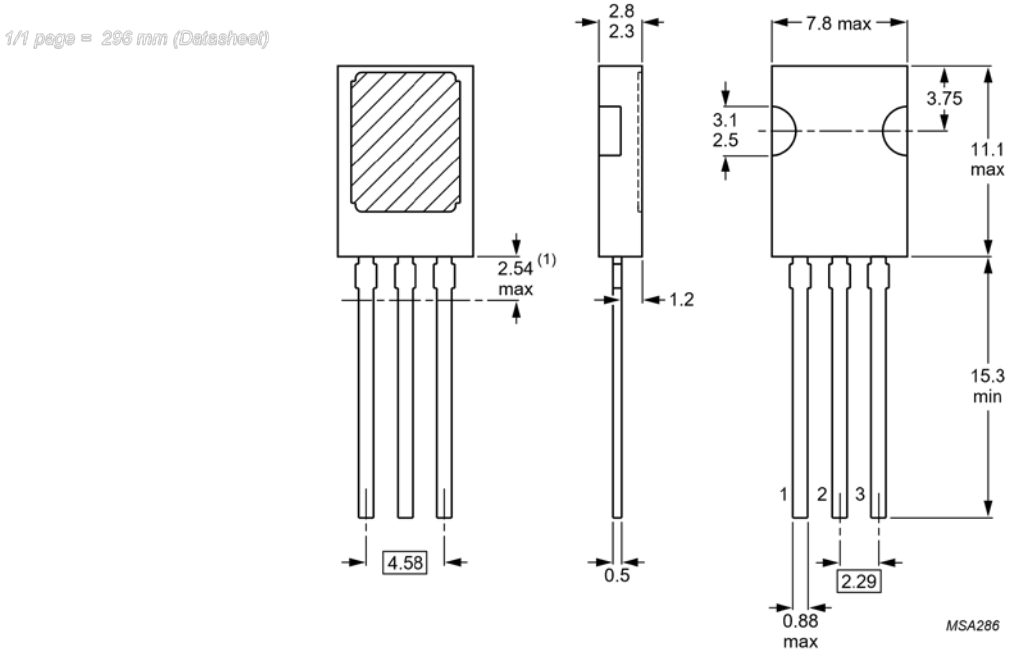

Fig.12 SOT82

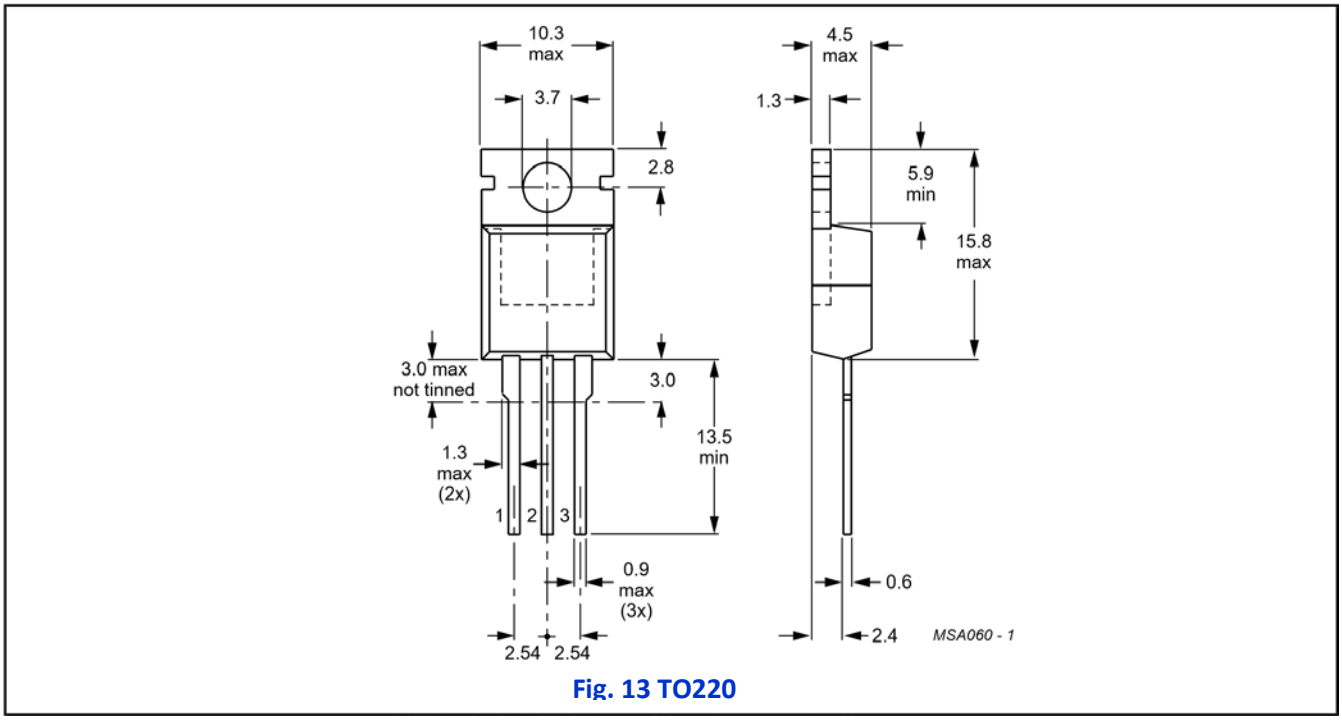

Fig. 13 TO220

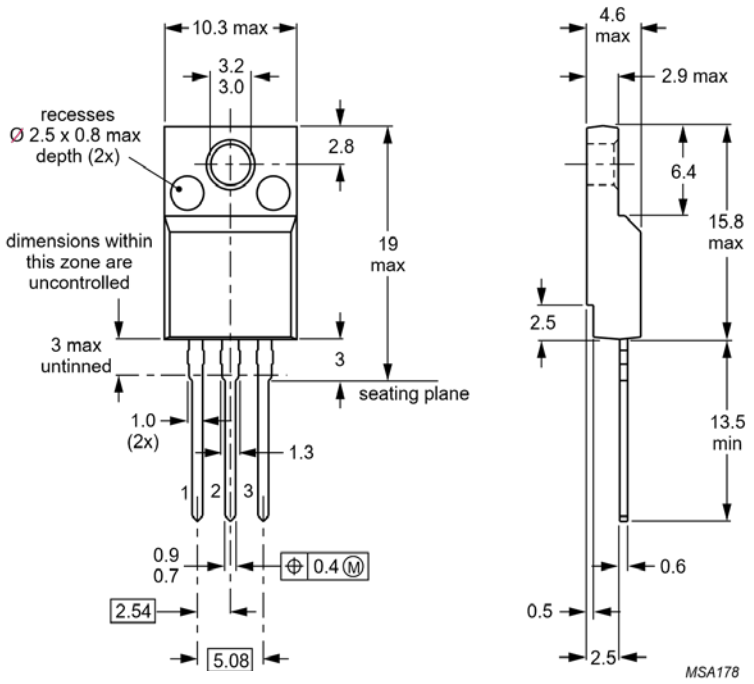

Fig. 14 TO220F

Summary of the 10 golden rules

1. To turn a thyristor (or triac) ON, a gate current ≥ I_{GT} must be applied until the load current is ≥ I_L. This condition must be met at the lowest expected operating temperature.

2. To turn off (commutate) a thyristor (or triac), the load current must be < I_H for enough time to allow a return to the blocking state. This condition must be met at the highest expected operating temperature.

3. When designing a triac triggering circuit, avoid triggering in the 3^+ quadrant (MT2-, G+) where possible.

4. To minimise noise pickup, keep gate connection length to a minimum.
   Take the return directly to MT1 (or cathode).
   If hard wired, use twisted pair or shielded cable.
   Fit a resistor of 1kΩ or less between gate and MT1.
   Fit a bypass capacitor in conjunction with a series resistor to the gate.
   Alternatively, use an insensitive series H triac.

5. Where high dV_D/dt or dV_{COM}/dt are likely to cause a problem, fit an RC snubber across MT1 and MT2. Where high dI_{COM}/dt is likely to cause a problem, fit an inductor of a few mH in series with the load. Alternatively, use a Hi-Com triac.

6. If the triac's V_{DRM} is likely to be exceeded during severe mains transients, employ one of the following measures:

   a. Limit high dI_T/dt with a non-saturable inductor of a few µH in series with the load.
   b. Use a MOV across the mains in combination with filtering on the supply side.

7. Healthy gate drive and avoiding 3^+ operation maximises the triac's dI_T/dt capability.

8. If the triac's dI_T/dt is likely to be exceeded, an air cored inductor of a few µH or an NTC thermistor should be fitted in series with the load. Alternatively, employ zero voltage turn-on for resistive loads.

9. Avoid mechanical stress to the triac when fitting it to the heatsink. Fix, then solder. Never pop rivet with the rivet mandrel on the tab side.

10. For long-term reliability, ensure that the $R_{th(j-a)}$ is low enough to keep the junction temperature within $T_{j(max)}$ for the highest expected ambient temperature.

Revision history

Rev	Date	Description
v.2	20190501	new company update
v.3	20193107	format update

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