

# DATA SHEET

## **BTA212X series D, E and F** Three quadrant triacs guaranteed commutation

Product specification

September 2018



**WeEn**  
WeEn Semiconductors

# Three quadrant triacs guaranteed commutation

# BTA212X series D, E and F

## GENERAL DESCRIPTION

Passivated guaranteed commutation triacs in a full pack, plastic envelope intended for use in motor control circuits or with other highly inductive loads. These devices balance the requirements of commutation performance and gate sensitivity. The "sensitive gate" E series and "logic level" D series are intended for interfacing with low power drivers, including micro controllers.

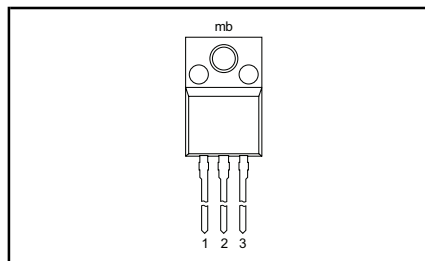
## QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
$V_{DRM}$	Repetitive peak off-state voltages	<b>600D</b> <b>600E</b> <b>600F</b> 600	- <b>800E</b> -	V
$I_{T(RMS)}$	RMS on-state current	12	12	A
$I_{TSM}$	Non-repetitive peak on-state current	95	95	A

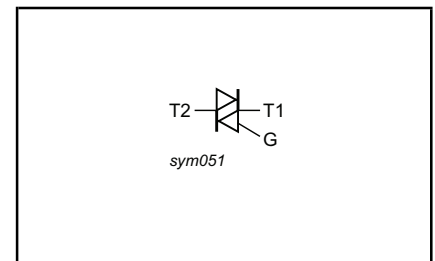
## PINNING - SOT186A

PIN	DESCRIPTION
1	main terminal 1
2	main terminal 2
3	gate
case	isolated

## PIN CONFIGURATION



## SYMBOL



## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
$V_{DRM}$	Repetitive peak off-state voltages		-	<b>-600</b> 600 <sup>1</sup>	<b>-800</b> 800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{hs} \leq 56^\circ C$	-	12		A
$I_{TSM}$	Non-repetitive peak on-state current	full sine wave; $T_j = 25^\circ C$ prior to surge	-	95		A
$I^2t$	$I^2t$ for fusing	$t = 20$ ms	-	105		A
$dl_T/dt$	Repetitive rate of rise of on-state current after triggering	$t = 16.7$ ms	-	45		A <sup>2</sup> s
		$t = 10$ ms	-	100		A/ $\mu$ s
		$I_{TM} = 20$ A; $I_G = 0.2$ A; $dl_G/dt = 0.2$ A/ $\mu$ s				
$I_{GM}$	Peak gate current		-	2		A
$P_{GM}$	Peak gate power		-	5		W
$P_{G(AV)}$	Average gate power	over any 20 ms period	-	0.5		W
$T_{stg}$	Storage temperature		-40	150		$^\circ C$
$T_j$	Operating junction temperature		-	125		$^\circ C$

<sup>1</sup> Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 15 A/ $\mu$ s.

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### ISOLATION LIMITING VALUE & CHARACTERISTIC

$T_{hs} = 25\text{ °C}$  unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{isol}$	R.M.S. isolation voltage from all three terminals to external heatsink	$f = 50\text{-}60\text{ Hz}$ ; sinusoidal waveform; R.H. $\leq 65\%$ ; clean and dustfree	-	-	2500	V
$C_{isol}$	Capacitance from T2 to external heatsink	$f = 1\text{ MHz}$	-	10	-	pF

### THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}hs}$	Thermal resistance junction to heatsink	full or half cycle with heatsink compound	-	-	4.0	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	without heatsink compound in free air	-	55	5.5	K/W

### STATIC CHARACTERISTICS

$T_j = 25\text{ °C}$  unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.			UNIT
				...D	...E	...F	
$I_{GT}$	Gate trigger current <sup>2</sup>	<b>BTA212X-</b>					
		$V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ T2+ G+	-	5	10	25	mA
		T2+ G-	-	5	10	25	mA
$I_L$	Latching current	$V_D = 12\text{ V}$ ; $I_{GT} = 0.1\text{ A}$ T2- G-	-	5	10	25	mA
		T2+ G+	-	15	25	30	mA
		T2+ G-	-	25	30	40	mA
		T2- G-	-	25	30	40	mA
$I_H$	Holding current	$V_D = 12\text{ V}$ ; $I_{GT} = 0.1\text{ A}$	-	15	25	30	mA
$V_T$	On-state voltage	$I_T = 17\text{ A}$	-	1.6			V
$V_{GT}$	Gate trigger voltage	$V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$	-	1.5			V
		$V_D = 400\text{ V}$ ; $I_T = 0.1\text{ A}$ ; $T_j = 125\text{ °C}$	0.25	-			V
$I_D$	Off-state leakage current	$V_D = V_{DRM(max)}$ ; $T_j = 125\text{ °C}$	-	0.5			mA

<sup>2</sup> Device does not trigger in the T2-, G+ quadrant.

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### DYNAMIC CHARACTERISTICS

$T_j = 25\text{ °C}$  unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.			MAX.	UNIT
			...D	...E	...F		
$dV_D/dt$	Critical rate of rise of off-state voltage	<b>BTA212X-</b> $V_{DM} = 67\% V_{DRM(max)}$ ; $T_j = 110\text{ °C}$ ; exponential waveform; gate open circuit	30	60	70	-	V/ $\mu$ s
$di_{com}/dt$	Critical rate of change of commutating current	$V_{DM} = 400\text{ V}$ ; $T_j = 125\text{ °C}$ ; $I_{T(RMS)} = 12\text{ A}$ ; $dV_{com}/dt = 10\text{ V}/\mu\text{s}$ ; gate open circuit	1.0	8.0	21	-	A/ms
$di_{com}/dt$	Critical rate of change of commutating current	$V_{DM} = 400\text{ V}$ ; $T_j = 125\text{ °C}$ ; $I_{T(RMS)} = 12\text{ A}$ ; $dV_{com}/dt = 0.1\text{ V}/\mu\text{s}$ ; gate open circuit	3.5	16	32	-	A/ms

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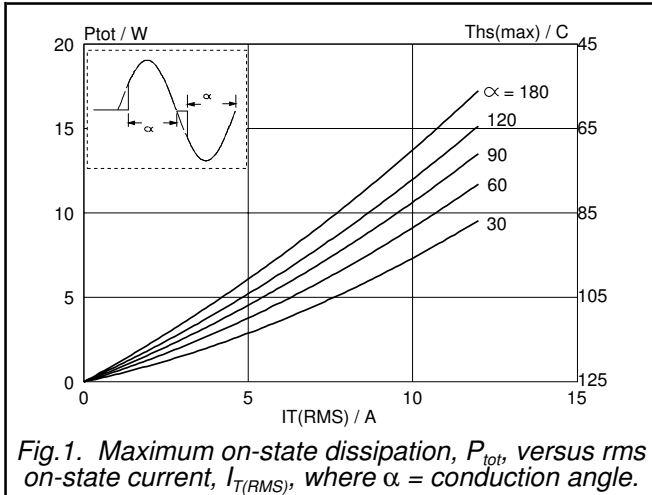


Fig.1. Maximum on-state dissipation,  $P_{tot}$ , versus rms on-state current,  $I_{T(RMS)}$ , where  $\alpha$  = conduction angle.

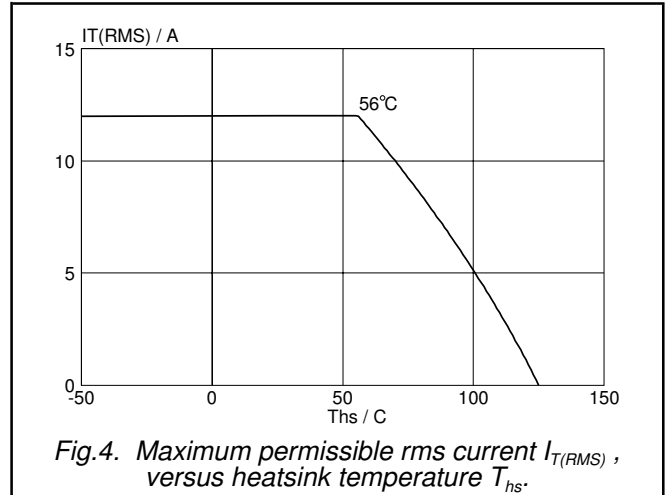


Fig.4. Maximum permissible rms current  $I_{T(RMS)}$ , versus heatsink temperature  $T_{hs}$ .

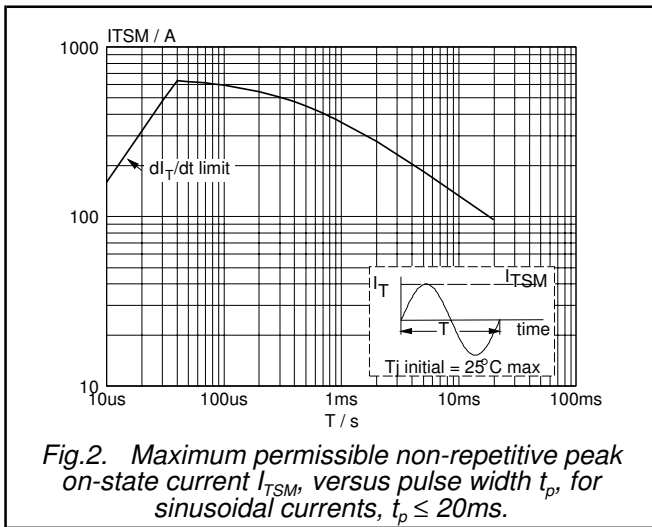


Fig.2. Maximum permissible non-repetitive peak on-state current  $I_{TSM}$ , versus pulse width  $t_p$ , for sinusoidal currents,  $t_p \leq 20$ ms.

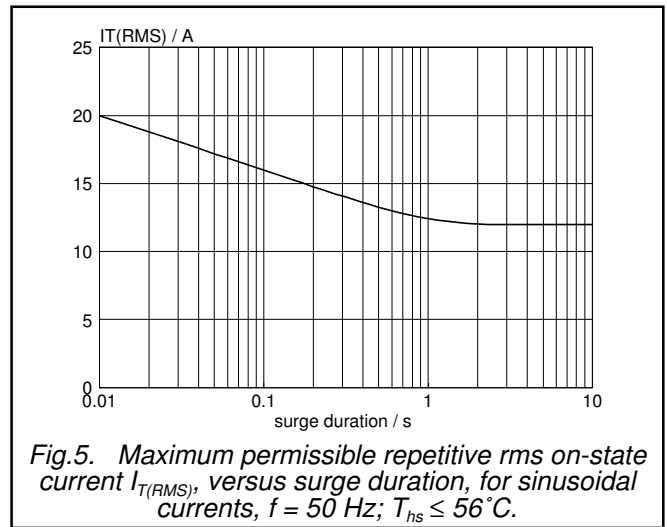


Fig.5. Maximum permissible repetitive rms on-state current  $I_{T(RMS)}$ , versus surge duration, for sinusoidal currents,  $f = 50$  Hz;  $T_{hs} \leq 56$  C.

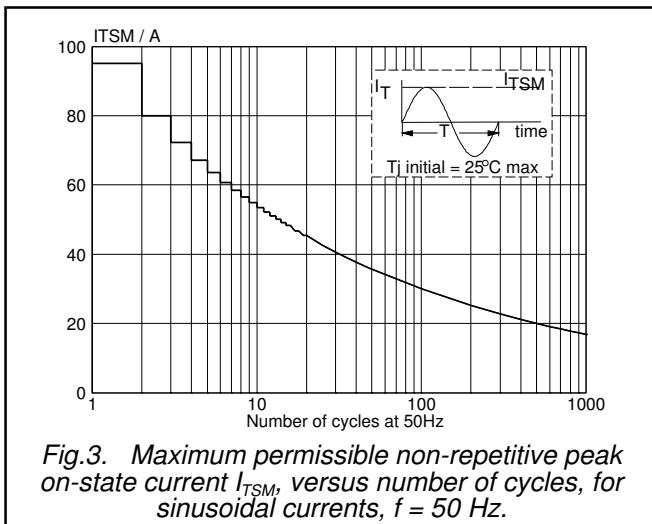


Fig.3. Maximum permissible non-repetitive peak on-state current  $I_{TSM}$ , versus number of cycles, for sinusoidal currents,  $f = 50$  Hz.

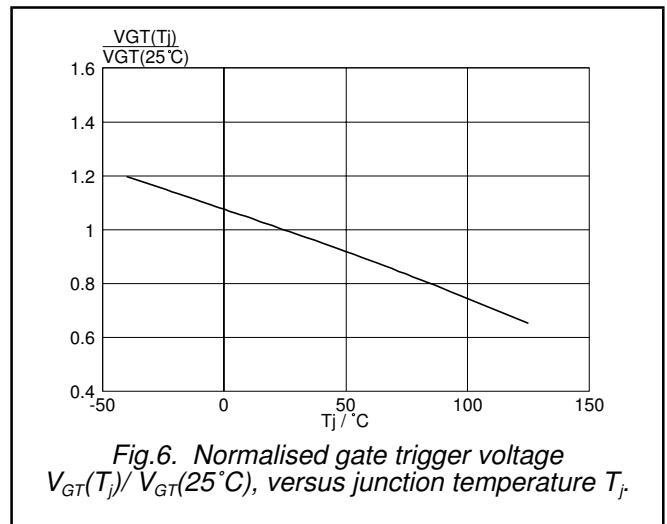
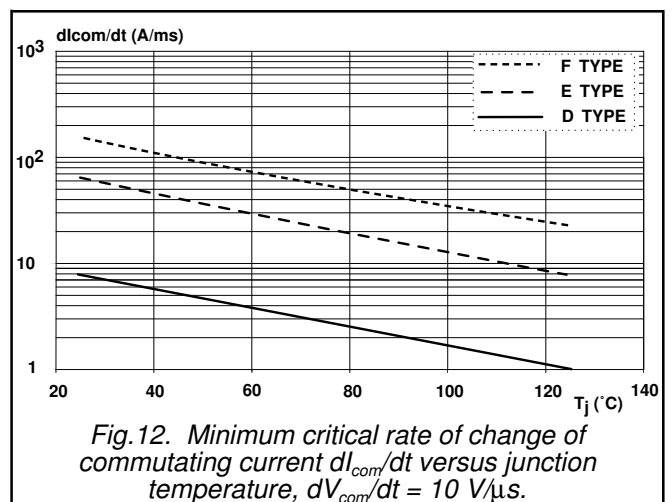
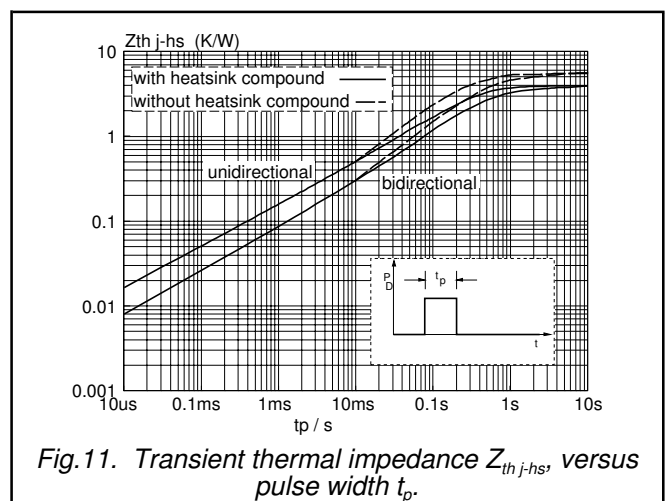
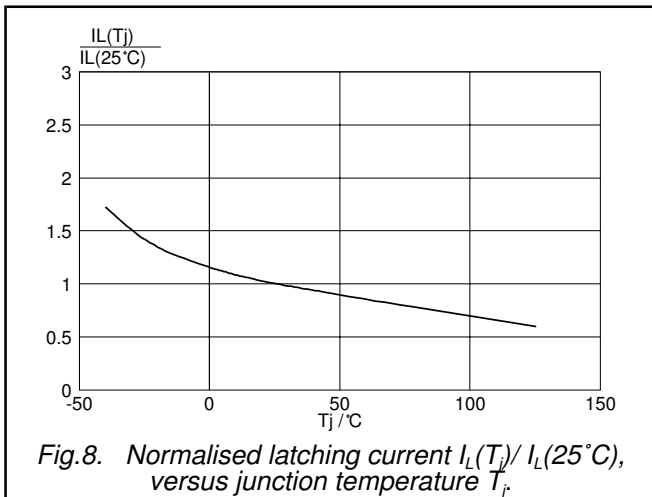
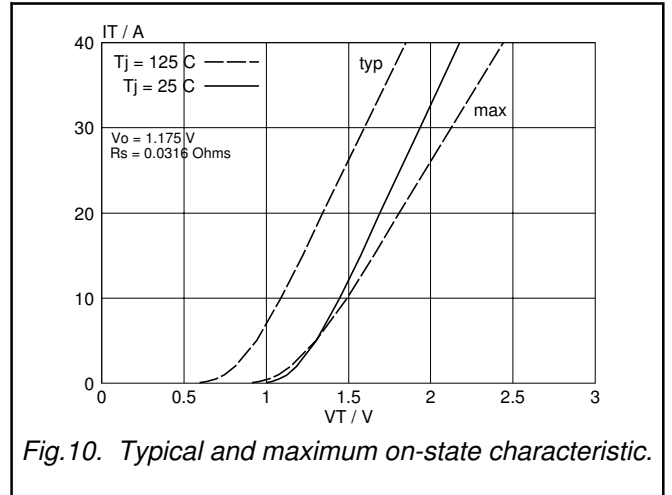
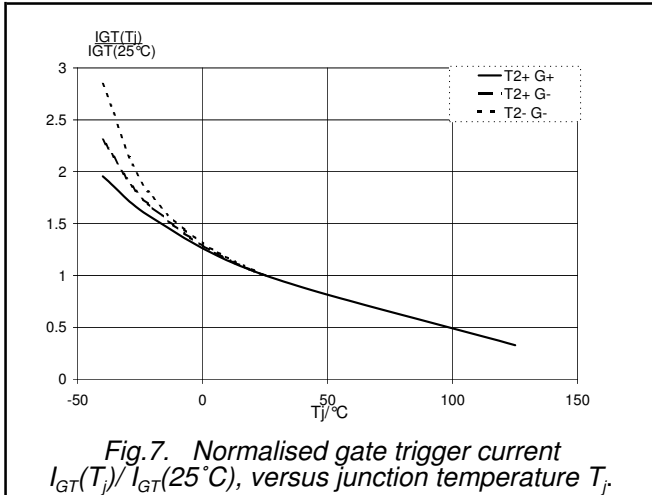


Fig.6. Normalised gate trigger voltage  $V_{GT}(T_j) / V_{GT}(25 C)$ , versus junction temperature  $T_j$ .

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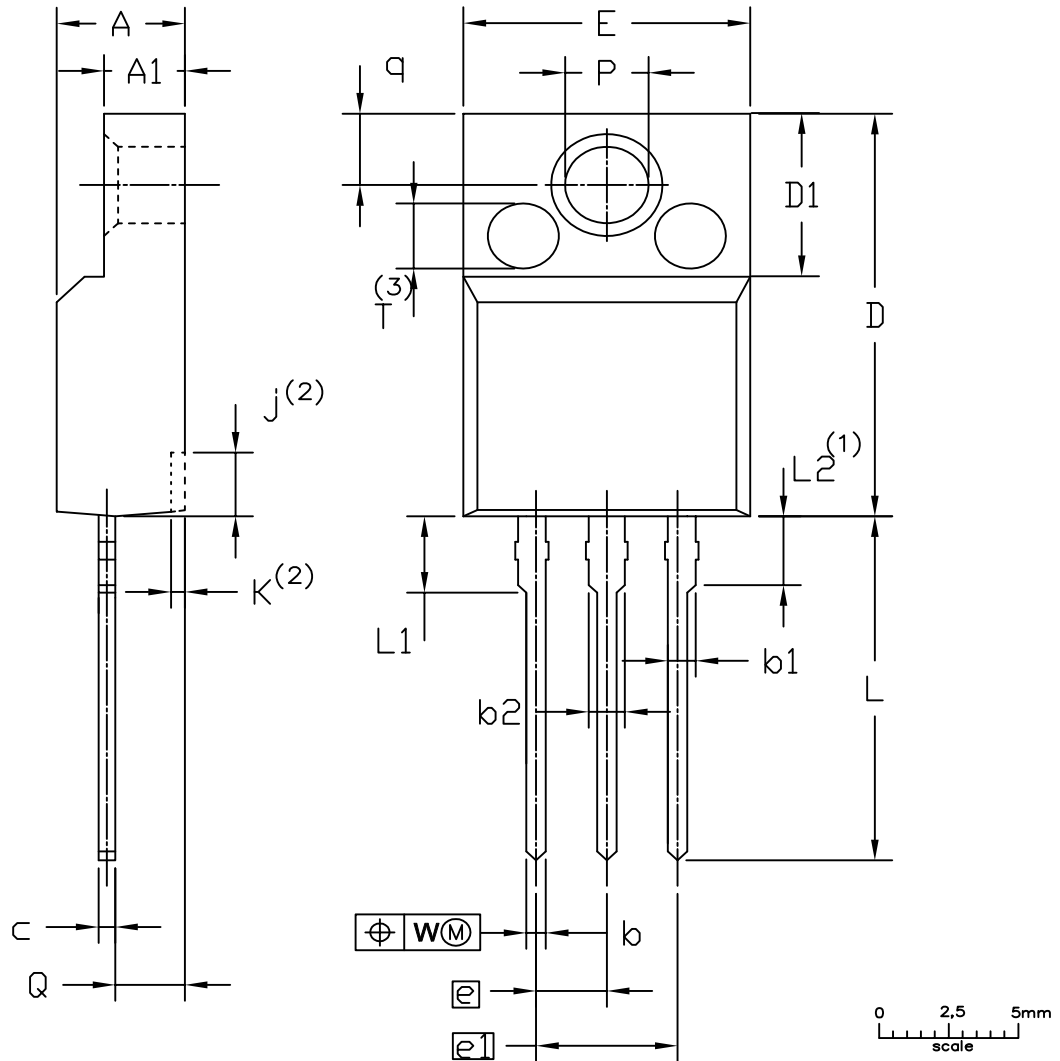
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**MECHANICAL DATA**

Plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3-lead TO-220 "full pack"

SOT186A



UNIT	A	A <sub>1</sub>	b	b <sub>1</sub>	b <sub>2</sub>	c	D	D <sub>1</sub>	E	e	e <sub>1</sub>	j <sup>(2)</sup>	k <sup>(2)</sup>	L	L <sub>1</sub>	L <sub>2</sub> <sup>(1)</sup> max.	P	Q	q	W	T <sup>(3)</sup>
mm	4.6	2.9	0.9	1.1	1.4	0.7	15.8	6.5	10.3			2.7	0.6	14.4	3.30		3.2	2.6	3.0		
	4.0	2.5	0.7	0.9	1.0	0.4	15.2	6.3	9.7	2.54	5.08	1.7	0.4	13.5	2.79	3	3.0	2.3	2.6	0.4	2.5

Notes

1. Terminal dimensions within this zone are uncontrolled
2. Dot lines area designs may vary
3. Eject pin mark is for reference only

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT186A		3 LEADS TO220F			2013-11-14

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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