

1. General description

AC Thyristor Triac power switch in a SOT404 (D2PAK) surface mountable plastic package with self-protective clamping capabilities against low and high energy transients.

2. Features and benefits

- Clamping structure ensuring safe high over-voltage withstand capability
- Pin compatible with standard triacs
- Full cycle AC conduction
- Over-voltage withstand capability to IEC 61000-4-5
- Planar passivated for voltage ruggedness and reliability
- Protective self turn-on capability for high energy transients
- Safe clamping capability for low energy over-voltage transients
- Less sensitive gate for high noise immunity
- Triggering in three quadrants only
- Very high immunity to false turn-on by dV/dt and IEC 61000-4-4 fast transient
- Enhanced dynamic performance
- Surface mountable package
- Package is RoHS compliant
- Package meets UL94V0 flammability requirement

3. Applications

- Fan motor circuits
- Highly inductive, resistive and safety loads
- Loads such as contactors, circuit breakers, valves, dispensers and door locks
- Pump motor circuits

4. Quick reference data

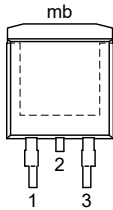
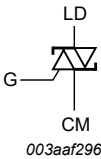
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	-	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{mb} \leq 109\text{ °C}$; Fig. 1 ; Fig. 2 ; Fig. 3	-	-	6	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(init)} = 25\text{ °C}$; $t_p = 16.7\text{ ms}$	-	-	66	A
		full sine wave; $T_{j(init)} = 25\text{ °C}$; $t_p = 20\text{ ms}$; Fig. 4 ; Fig. 5	-	-	60	A
T_j	junction temperature		-	-	125	°C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{PP}	peak pulse voltage	T _j = 25 °C; non-repetitive, off-state; Fig. 6	-	-	2	kV
Static characteristics						
I _{GT}	gate trigger current	V _D = 12 V; I _T = 100 mA; LD+ G+; T _j = 25 °C; Fig. 8	5	-	35	mA
		V _D = 12 V; I _T = 100 mA; LD+ G-; T _j = 25 °C; Fig. 8	5	-	35	mA
		V _D = 12 V; I _T = 100 mA; LD- G-; T _j = 25 °C; Fig. 8	5	-	35	mA
I _H	holding current	V _D = 12 V; T _j = 25 °C; Fig. 10	-	-	40	mA
V _T	on-state voltage	I _T = 8 A; T _j = 25 °C; Fig. 11	-	-	1.65	V
V _{CL}	clamping voltage	I _{CL} = 0.1 mA; t _p = 1 ms; T _j = 25 °C	800	-	-	V
Dynamic characteristics						
dV _D /dt	rate of rise of off-state voltage	V _{DM} = 536 V; T _j = 125 °C; (V _{DM} = 67% of V _{DRM}); exponential waveform; gate open circuit	1500	-	-	V/μs
di _{com} /dt	rate of change of commutating current	V _D = 400 V; T _j = 125 °C; I _{T(RMS)} = 6 A; dV _{com} /dt = 20 V/μs; (snubberless condition); gate open circuit	12	-	-	A/ms
		V _D = 400 V; T _j = 125 °C; I _{T(RMS)} = 6 A; dV _{com} /dt = 10 V/μs; gate open circuit	15	-	-	A/ms
		V _D = 400 V; T _j = 125 °C; I _{T(RMS)} = 6 A; dV _{com} /dt = 1 V/μs; gate open circuit	20	-	-	A/ms

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	CM	common	 <p>D2PAK (SOT404A)</p>	 <p>003aaf296</p>
2	LD	load		
3	G	gate		
mb	LD	mounting base; load		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
ACTT6B-800CN	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404A

7. Marking

Table 4. Marking codes

Type number	Marking code
ACTT6B-800CN	ACTT6B-800CN

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{mb} \leq 109\text{ }^{\circ}\text{C}$; Fig. 1 ; Fig. 2 ; Fig. 3	-	6	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(\text{init})} = 25\text{ }^{\circ}\text{C}$; $t_p = 16.7\text{ ms}$	-	66	A
		full sine wave; $T_{j(\text{init})} = 25\text{ }^{\circ}\text{C}$; $t_p = 20\text{ ms}$; Fig. 4 ; Fig. 5	-	60	A
I^2t	I^2t for fusing	$t_p = 10\text{ ms}$; sine-wave pulse	-	18	A^2s
di_T/dt	rate of rise of on-state current	$I_G = 70\text{ mA}$	-	100	$\text{A}/\mu\text{s}$
I_{GM}	peak gate current	$t = 20\text{ }\mu\text{s}$	-	2	A
P_{GM}	peak gate power		-	5	W
$P_{G(AV)}$	average gate power	over any 20 ms period	-	0.5	W
T_j	junction temperature		-	125	$^{\circ}\text{C}$
V_{PP}	peak pulse voltage	$T_j = 25\text{ }^{\circ}\text{C}$; non-repetitive, off-state; Fig. 6	-	2	kV

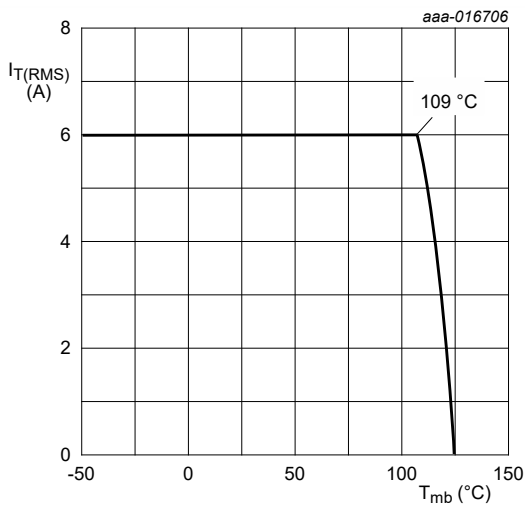


Fig. 1. RMS on-state current as a function of mounting base temperature; maximum values

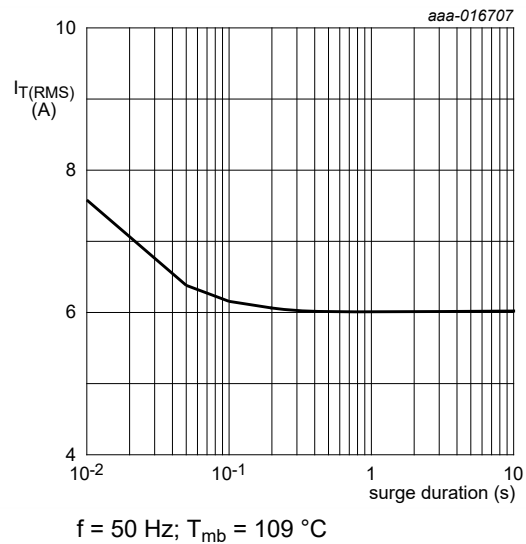


Fig. 2. RMS on-state current as a function of surge duration; maximum values

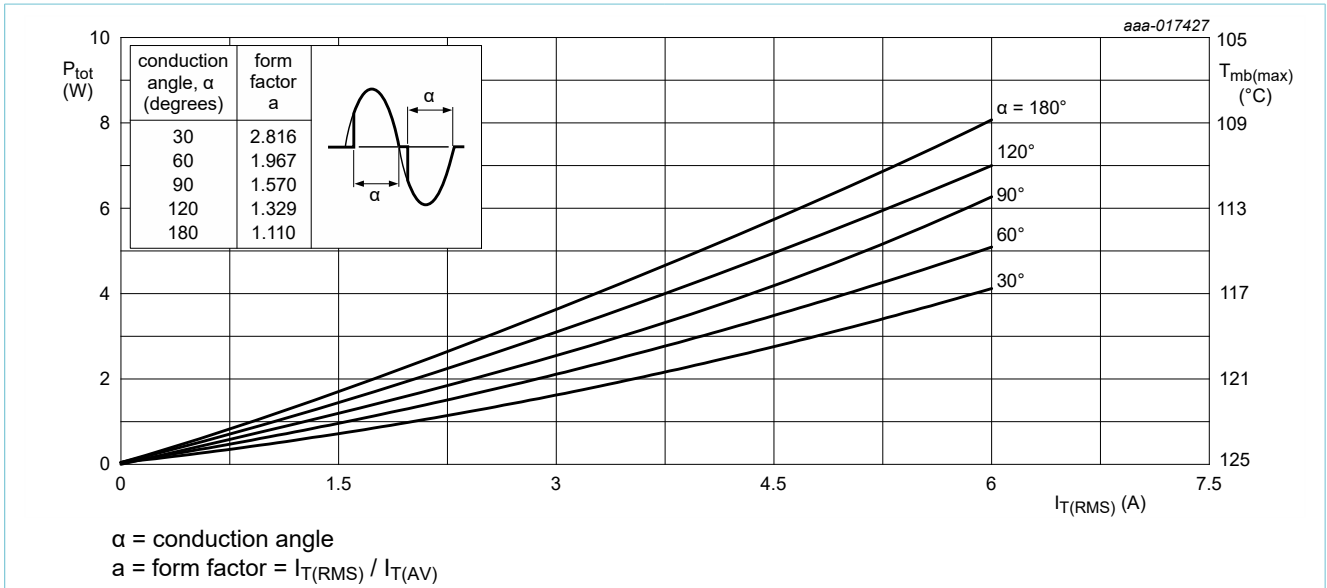


Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values

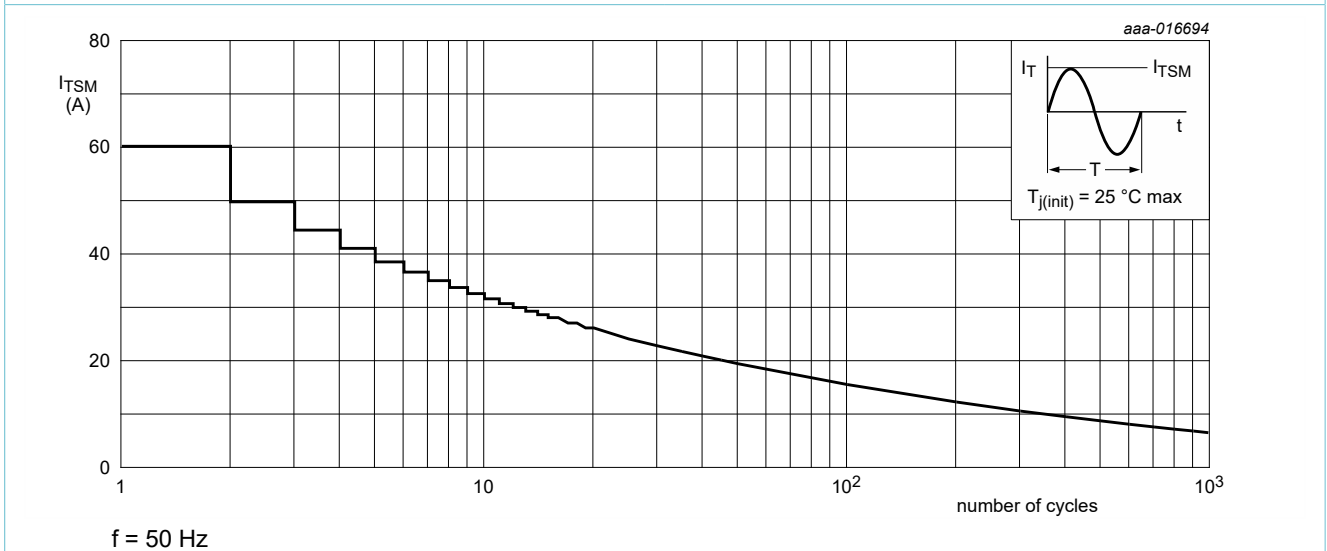


Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values

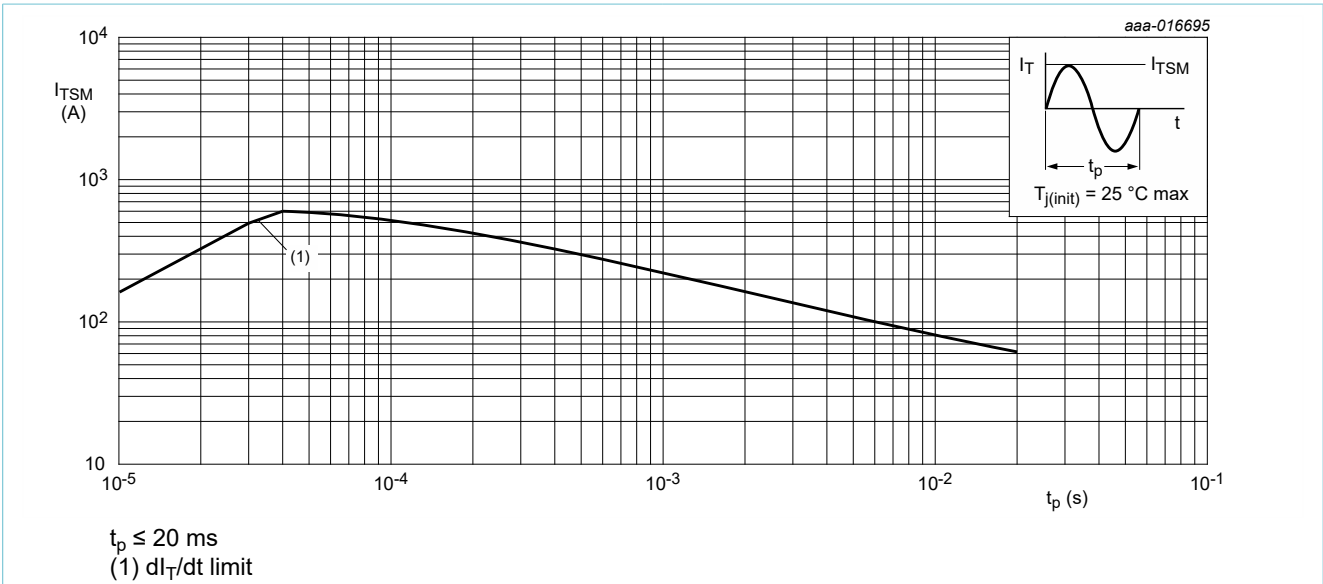


Fig. 5. Non-repetitive peak on-state current as a function of pulse width; maximum values

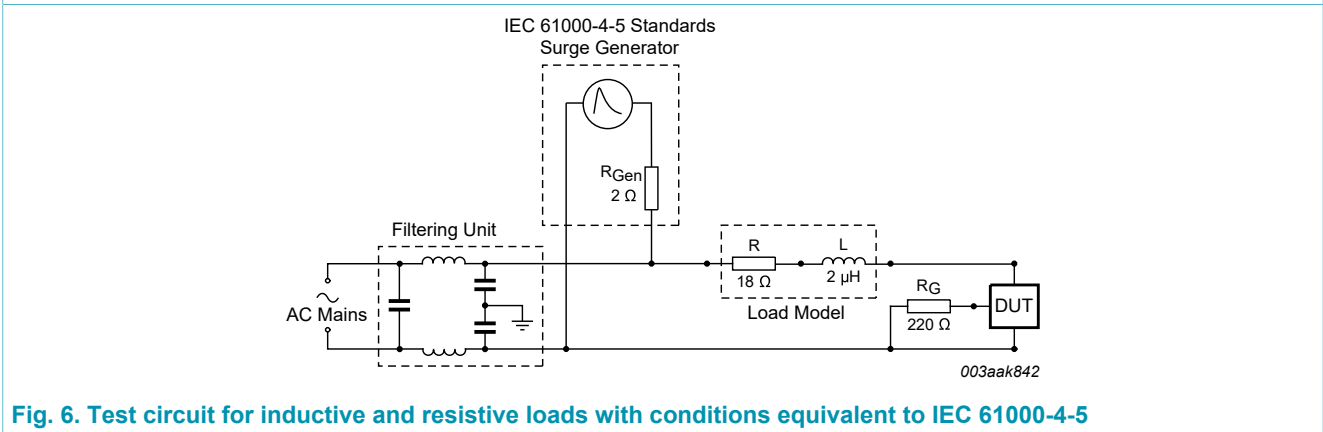
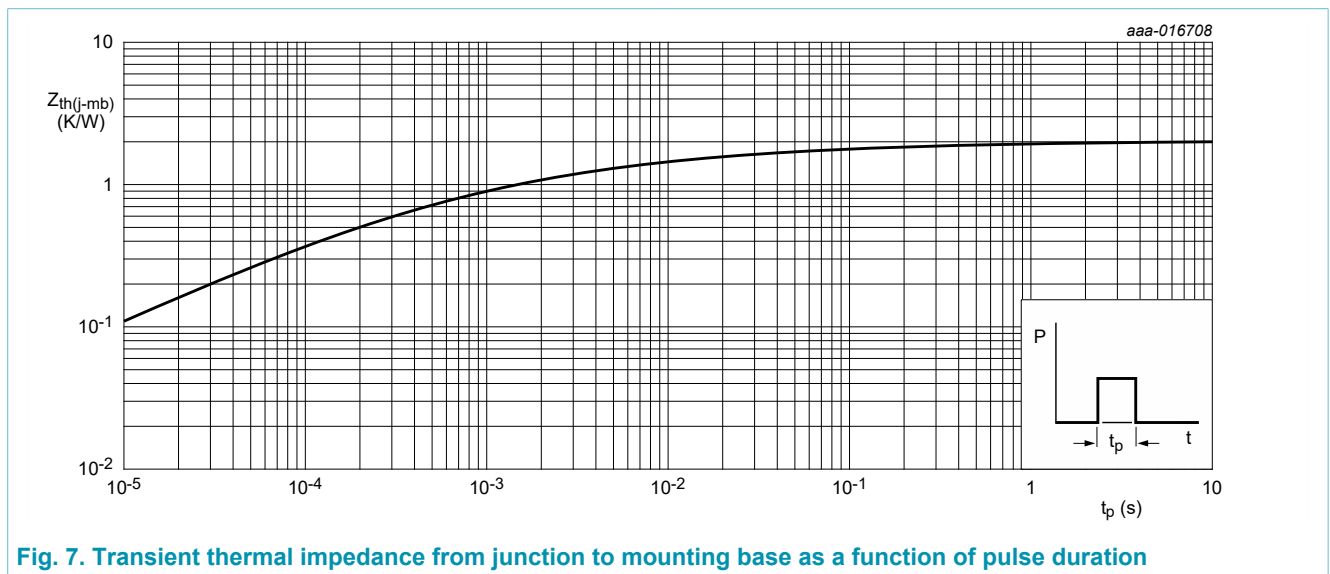


Fig. 6. Test circuit for inductive and resistive loads with conditions equivalent to IEC 61000-4-5

9. Thermal characteristics

Table 6. Thermal characteristics

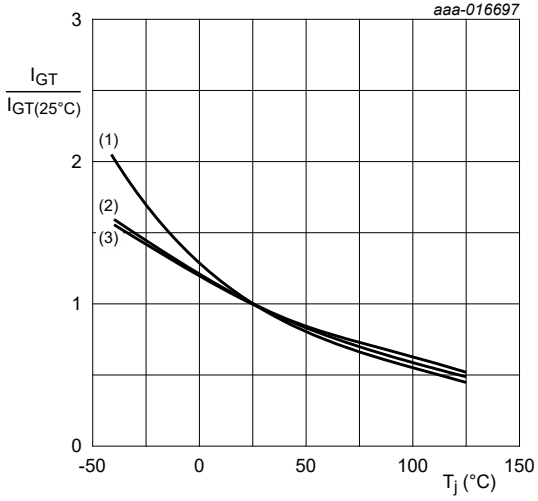
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R _{th(j-mb)}	thermal resistance from junction to mounting base	half cycle	-	-	2.4	K/W
		full cycle; Fig. 7	-	-	2	K/W
R _{th(j-a)}	thermal resistance from junction to ambient free air	printed circuit board (FR4) mounted	-	55	-	K/W



10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I_{GT}	gate trigger current	$V_D = 12\text{ V}$; $I_T = 100\text{ mA}$; LD+ G+; $T_j = 25\text{ °C}$; Fig. 8	5	-	35	mA
		$V_D = 12\text{ V}$; $I_T = 100\text{ mA}$; LD+ G-; $T_j = 25\text{ °C}$; Fig. 8	5	-	35	mA
		$V_D = 12\text{ V}$; $I_T = 100\text{ mA}$; LD- G-; $T_j = 25\text{ °C}$; Fig. 8	5	-	35	mA
I_L	latching current	$V_D = 12\text{ V}$; $I_G = 100\text{ mA}$; LD+ G+; $T_j = 25\text{ °C}$; Fig. 9	-	-	50	mA
		$V_D = 12\text{ V}$; $I_G = 100\text{ mA}$; LD+ G-; $T_j = 25\text{ °C}$; Fig. 9	-	-	75	mA
		$V_D = 12\text{ V}$; $I_G = 100\text{ mA}$; LD- G-; $T_j = 25\text{ °C}$; Fig. 9	-	-	50	mA
I_H	holding current	$V_D = 12\text{ V}$; $T_j = 25\text{ °C}$; Fig. 10	-	-	40	mA
V_T	on-state voltage	$I_T = 8\text{ A}$; $T_j = 25\text{ °C}$; Fig. 11	-	-	1.65	V
V_{GT}	gate trigger voltage	$V_D = 12\text{ V}$; $I_T = 100\text{ mA}$; $T_j = 25\text{ °C}$; Fig. 12	-	0.8	1	V
		$V_D = 400\text{ V}$; $I_T = 100\text{ mA}$; $T_j = 125\text{ °C}$; Fig. 12	0.2	0.45	-	V
I_D	off-state current	$V_D = 800\text{ V}$; $T_j = 25\text{ °C}$	-	-	10	μA
		$V_D = 800\text{ V}$; $T_j = 125\text{ °C}$	-	-	0.5	mA
V_{CL}	clamping voltage	$I_{CL} = 0.1\text{ mA}$; $t_p = 1\text{ ms}$; $T_j = 25\text{ °C}$	800	-	-	V
Dynamic characteristics						
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 536\text{ V}$; $T_j = 125\text{ °C}$; ($V_{DM} = 67\%$ of V_{DRM}); exponential waveform; gate open circuit	1500	-	-	V/ μs
dI_{com}/dt	rate of change of commutating current	$V_D = 400\text{ V}$; $T_j = 125\text{ °C}$; $I_{T(RMS)} = 6\text{ A}$; $dV_{com}/dt = 20\text{ V}/\mu\text{s}$; (snubberless condition); gate open circuit	12	-	-	A/ms
		$V_D = 400\text{ V}$; $T_j = 125\text{ °C}$; $I_{T(RMS)} = 6\text{ A}$; $dV_{com}/dt = 10\text{ V}/\mu\text{s}$; gate open circuit	15	-	-	A/ms
		$V_D = 400\text{ V}$; $T_j = 125\text{ °C}$; $I_{T(RMS)} = 6\text{ A}$; $dV_{com}/dt = 1\text{ V}/\mu\text{s}$; gate open circuit	20	-	-	A/ms



- (1) T2- G-
- (2) T2+ G-
- (3) T2+ G+

Fig. 8. Normalized gate trigger current as a function of junction temperature

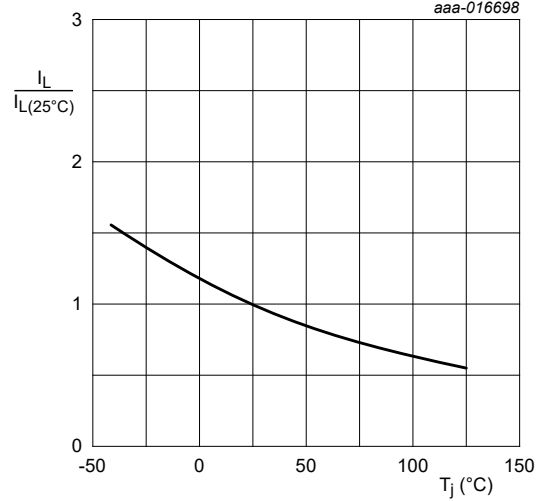


Fig. 9. Normalized latching current as a function of junction temperature

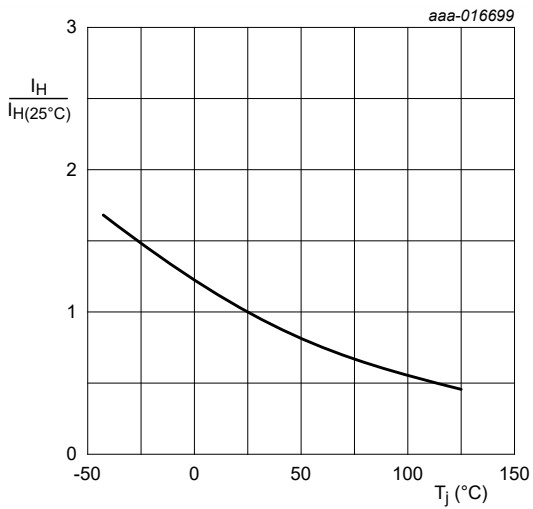
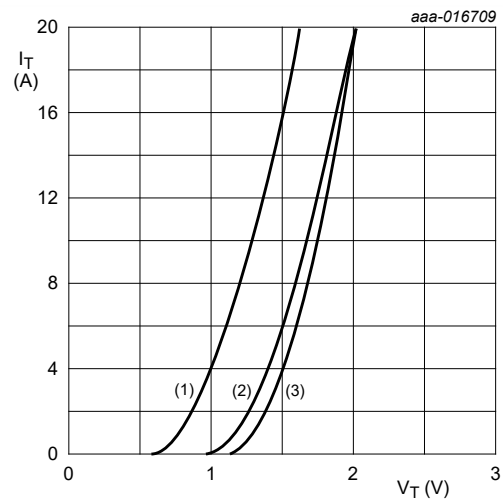


Fig. 10. Normalized holding current as a function of junction temperature



$V_o = 1.212 \text{ V}; R_s = 0.041 \Omega$

- (1) $T_j = 125^\circ\text{C}$; typical values
- (2) $T_j = 125^\circ\text{C}$; maximum values
- (3) $T_j = 25^\circ\text{C}$; maximum values

Fig. 11. On-state current as a function of on-state voltage

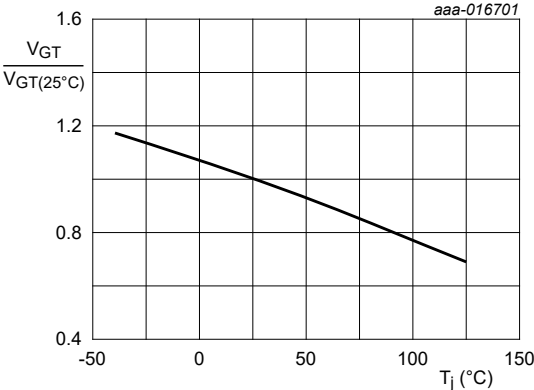
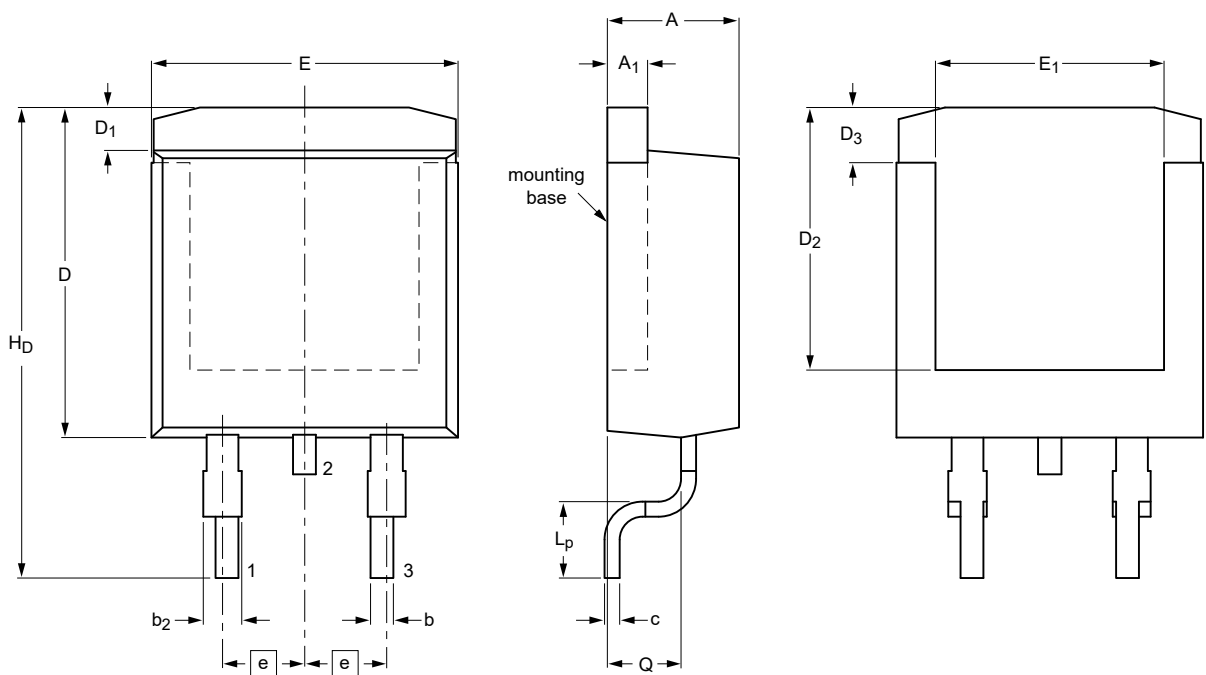


Fig. 12. Normalized gate trigger voltage as a function of junction temperature

11. Package outline

Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped) SOT404A



Dimensions (mm are the original dimensions)

Unit	A	A ₁	b	b ₂	c	D _{max}	D ₁	D ₂	D ₃	E	E ₁	e	H _D	L _p	Q
max	4.5	1.40	0.85	1.45	0.64	11	1.6	8.6	1.85	10.3	8.1	2.54	15.8	2.9	2.6
nom															
min	4.1	1.27	0.60	1.05	0.46		1.2	8.0	1.40	9.7	7.6		14.8	2.1	2.2

sot404a_po

Outline version	References			European projection	Issue date
	IEC	JEDEC	JEITA		
SOT404A					13-02-28 13-03-12

Fig. 13. Package outline D2PAK (SOT404A)

12. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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