AN10805

Surface mounted thyristors

Rev. 01 — 21 April 2009 **Application note**

Document information

Info	Content
Keywords	Surface mounted thyristors, soldering (reflow, wave), SMT/SMD, package types (SOT223, SOT404, SOT428), power devices
Abstract	The electronics industry faces a growing need for end-product miniaturization and cost reduction. To meet these needs, designers are specifying Surface-Mount Technology (SMT) with increasing regularity. Initially aimed at low-power and small signal components, the emphasis is now moving to total surface-mount solutions including power devices. This document details the surface-mount package options and their achievable thermal performances with standard PCBs without special heatsink provisions.

Revision history

Rev	Date	Description
01	20090421	Updated to meet NXP Semiconductors house style and rewritten.

Contact information

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1. Introduction

There is an ever-growing need in the electronics industry for miniaturization and cost reduction of the end product. In order to satisfy these requirements, designers are specifying Surface-Mount Technology (SMT) with increasing regularity. At first their attentions were aimed at the low power and small signal components. Now their attentions are turning towards the power devices in order to give them total surface-mount solutions.

The increased miniaturization is possible because surface mounted power semiconductors occupy less board area than through-hole-mounted devices on heatsinks. Cost reduction is possible due to the faster and simpler assembly that result when ALL components are surface mounted.

The availability of a wide range of package sizes permits continuous power dissipations ranging from 0.5 W to 2 W on standard Printed-Circuit Boards (PCB). Higher power dissipations are achievable if special heatsink provisions are made on the PCB. Some examples of these include:

- A grid of solder vias to a pad on the reverse side of the PCB
- A PCB-mounted heatsink on one or both sides
- An aluminium-cored PCB
- Fan-assisted cooling

2. Surface-mount solutions from NXP Semiconductors

NXP Semiconductors has developed a full range of surface-mount power packages for its entire range of triacs and Silicon Controlled Rectifiers (SCR). The assembly materials and technology used are not simply adapted from the pre-existing through-hole-mounting package technology; they are unique to SMT.

Every new SMT device is subjected to rigorous testing which originates from stringent automotive requirements. This consists of full reliability testing after three surface mounting operations on printed circuit boards. No failures will be generated. This gives the best assurance of reliable end products.

This technical publication will present the surface-mount packages and show what thermal performances can be achieved on standard PCBs without special heatsinking arrangements.

3. SOT223

SOT223 (Figure 1) is the smallest SMT power package presented in this publication. The mechanical design has been optimized for maximum ease and versatility of surface mounting, and maximum long-term reliability in the application. It will provide the minimum cost of ownership to the Original Equipment Manufacturer when initial purchase costs, handling costs and final assembly costs are added together.

The three legs and the heatsink tab emerge sideways from the edge of the plastic body, where they are formed to bring them into contact with the PCB for soldering to the pads. The center leg and the larger heatsink tab on the opposite side of the package are internally connected.

The main tab and the three legs emerge from the edge of the plastic package and are formed before they make contact with the PCB. This allows a certain degree of safe PCB movement relative to the device as the assembly expands and contracts during soldering and during circuit operation.

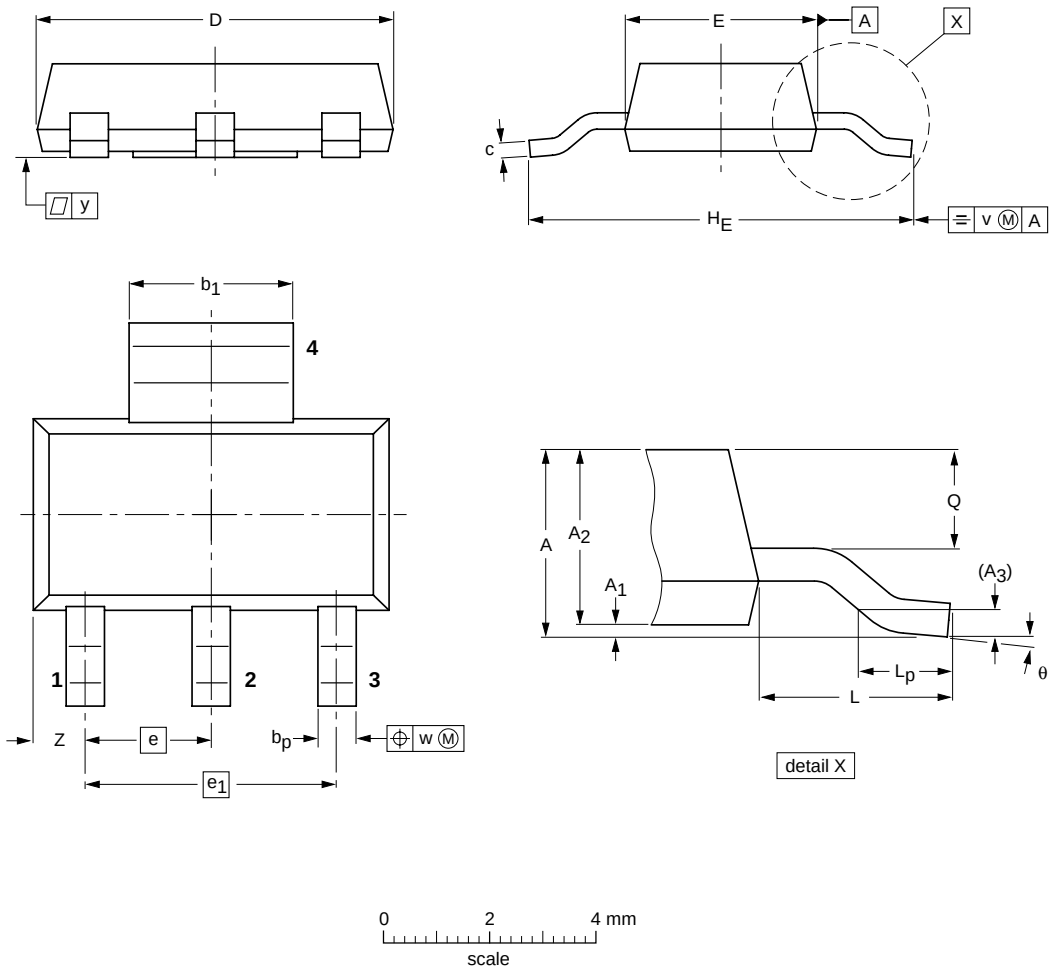
Since the device's die pad is not in direct contact with the PCB solder pad, differential movement caused by different coefficients of expansion can be accommodated without excessive fatigue stress to the solder joints. The more extreme condition of stresses being transmitted to the die, causing it to crack, is also minimized with this package design.

3.1 SOT223 soldering

When soldering most SMT power packages, a reflow process must be used. However, for SOT223, it is also feasible to use wave soldering if required. Wave soldering is possible because the small size of the package minimizes the size of the "shadow" on the downstream side of the solder flow. Perhaps more importantly, the exposed nature of the solder connections around the periphery of the package, and their relatively low thermal capacities, mean that full solder wetting is easily possible with wave soldering. The good visibility of the solder joints allows full inspection for quality after assembly.

Figure 2 and Figure 3 show the recommended SOT223 footprints for reflow soldering and for wave soldering

SO4: plastic small outline package; 4 leads; body width 3.5 mm **SOT223-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	b_1	c	$D^{(1)}$	$E^{(1)}$	e	e_1	H_E	L	L_p	Q	v	w	y	Z	θ
mm	1.8	0.10 0.02	1.7 1.5	0.25	0.85 0.65	3.15 2.95	0.35 0.25	6.7 6.3	3.7 3.3	2.3	4.6	7.3 6.7	1.75	1.02 0.62	1.0 0.8	0.2	0.1	0.1	1.2 0.7	10° 0°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT223-1		TO-261				~~99-12-15~~ 03-02-19

Fig 1. Package outline SOT223

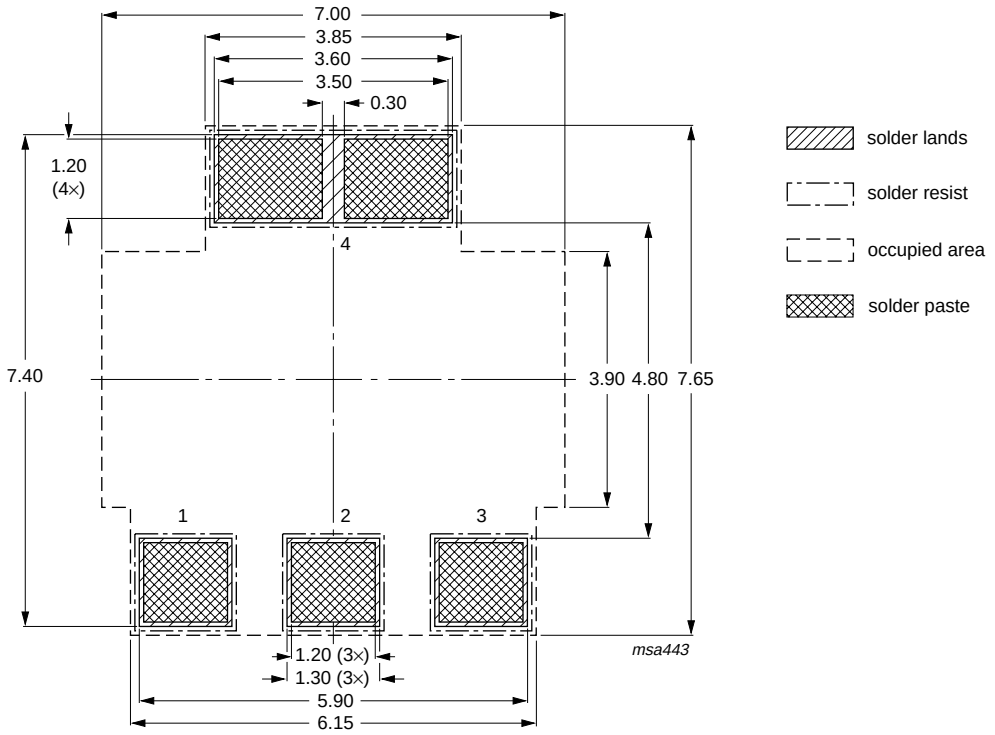


Fig 2. Reflow soldering footprint (SOT223)

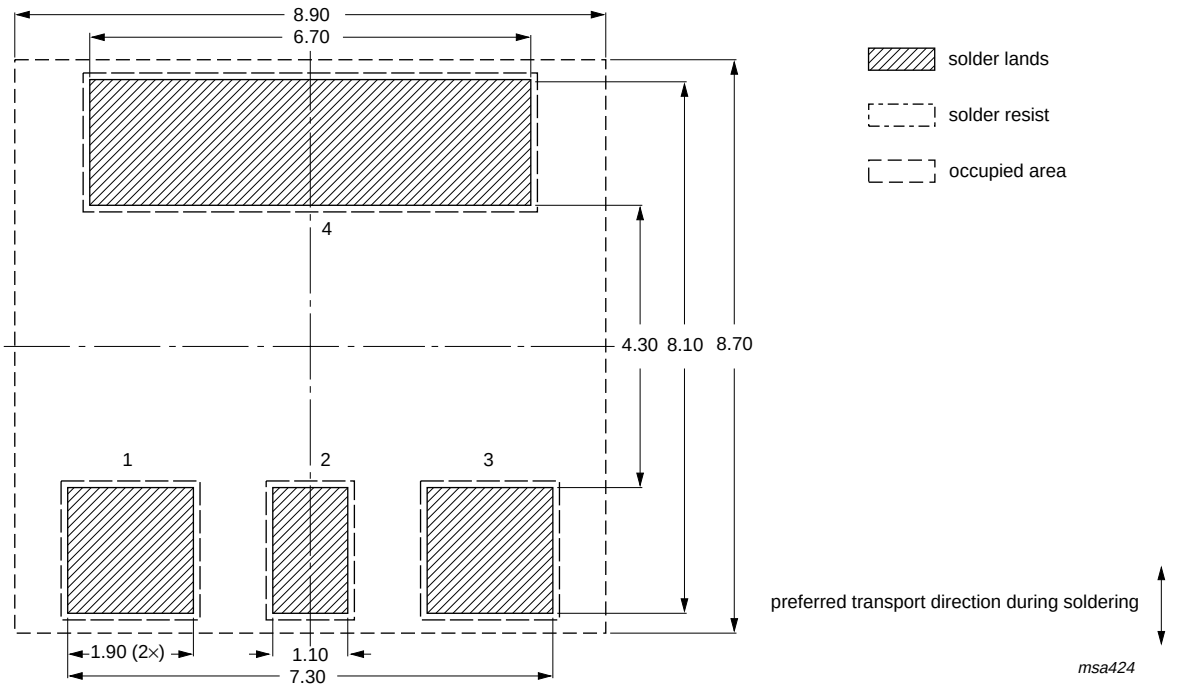


Fig 3. Wave soldering footprint (SOT223)

4. SOT428

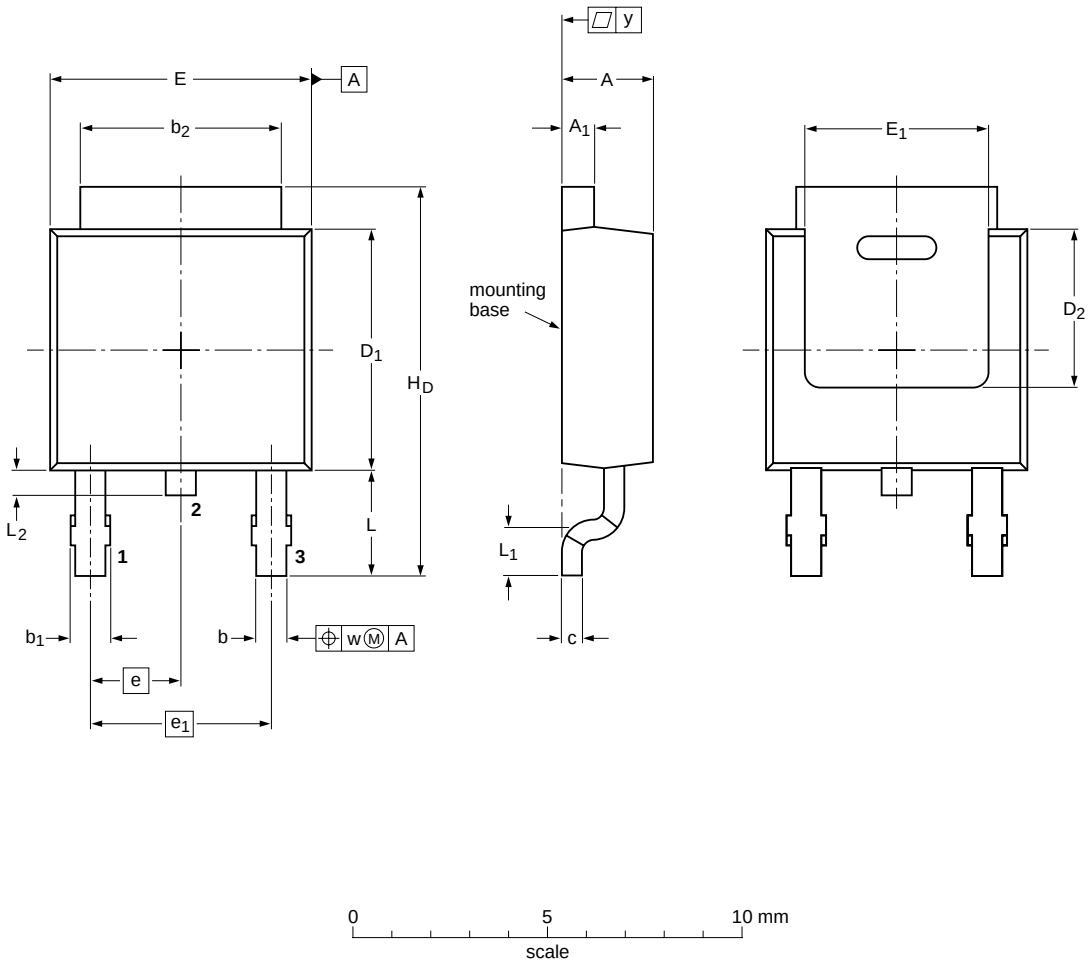
SOT428 (Figure 4, also known as TO252 and DPAK) occupies an area on the PCB that is not much larger than the area required for SOT223. Indeed, it can be soldered to a universal SOT223 and SOT428 pad layout. Figure 5 and Figure 7 show the pad and relative component sizes. The main pad area of 20 mm^2 is the minimum practical pad size for SOT428.

SOT428 has three legs, which emerge from one edge of the plastic body. The center leg is cropped off close to the plastic, so it is not used for electrical connection. The "center leg connection" is made from the device's metal mounting base to the main PCB pad. The two outer legs are formed to bring them into contact with the PCB pads for soldering.

4.1 SOT428 soldering

This surface-mount package features a relatively large solder area (compared to SOT223), which is hidden after assembly. In this case, wave soldering cannot be relied upon to wet the joint sufficiently because the mating surfaces between the main PCB pad and the device are hidden. It is therefore necessary to use a reflow soldering method for packages of this design. Figure 6 shows typical SOT428 solder pad dimensions.

Plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped) **SOT428**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	b_1	b_2	c	D_1	D_2 min	E	E_1 min	e	e_1	H_D	L	L_1 min	L_2	w	y max
mm	2.38 2.22	0.93 0.46	0.89 0.71	1.1 0.9	5.46 5.00	0.56 0.20	6.22 5.98	4.0	6.73 6.47	4.45	2.285	4.57	10.4 9.6	2.95 2.55	0.5	0.9 0.5	0.2	0.2

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT428		TO-252	SC-63			~~06-02-14~~ 06-03-16

Fig 4. Package outline SOT428

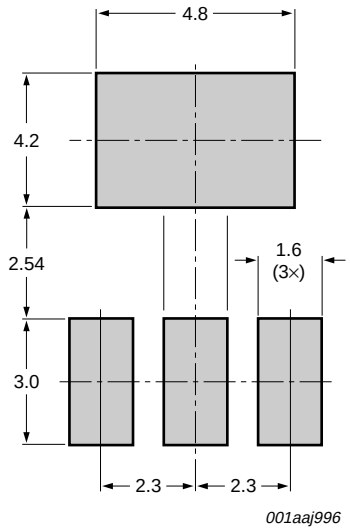


Fig 5. Universal SOT223 and SOT428 pad layout

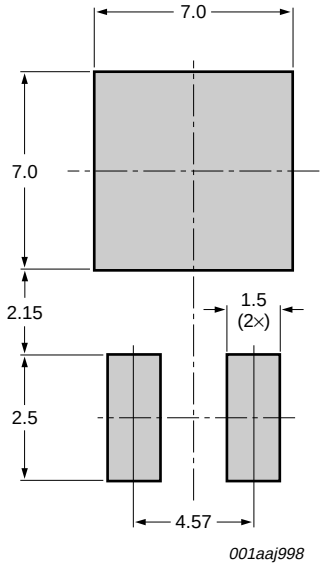


Fig 6. SOT428 pad layout

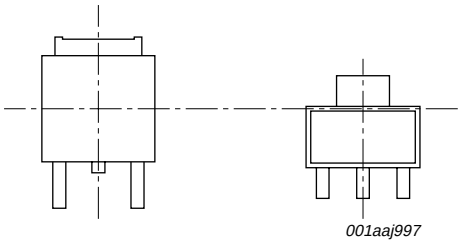


Fig 7. SOT223 and SOT428 relative package sizes

4.2 SOT428 design features for surface mounting

It is well known among power semiconductor manufacturers that the larger a surface mounted power semiconductor is, the more vulnerable it is to die stresses during manufacture and during the surface mounting process. This can result in a significant percentage of rejects due to die cracking.

Experience has shown that it is not possible to use the same manufacturing techniques for surface-mount devices as are used for through-hole devices. Unacceptable failure rates will certainly be the result, either during manufacture, during surface mounting or during prolonged thermal cycling in the application.

NXP Semiconductors has spent a long time perfecting its SOT428 package before releasing it onto the market so that these pitfalls can be avoided. Described below are some of the special design features that ensure successful manufacture and long-term reliable operation in the customer's application.

- The package is moulded using a low stress epoxy plastic in order to minimize the bending force on the mounting base as curing takes place. Less bending of the mounting base means less die stress.

- A thick copper mounting base of 0.93 mm maximum thickness is used to further inhibit any tendency for bending of the mounting base.
- A low stress soft solder is used for die bonding. The amount of "give" in the solder accommodates differential expansions and minimizes die stress
- A new technique has been developed to accurately control the thickness and positioning of the die-attach solder on the die pad. This guarantees optimum die bonding over the complete die area every time without unsoldered areas or excess solder. The benefit of this is to offer the best long-term reliability under thermal stress and the minimum junction-to-mounting base thermal resistance
- Special locking features are used to lock the epoxy to the metal to improve hermeticity. These features have been carefully optimized to provide good hermeticity while avoiding excessive die stress during differential expansion.
- A bare copper die pad is used for best adhesion of the epoxy to the metal. This promotes good hermeticity.
- The footprint is compatible with JEDEC industry standard layouts.
- The co-planarity of leads to seating plane and leads to leads meets stringent industry standards.
- A fully automatic high volume production line is used which takes in the raw components at its input and delivers assembled, 100 % tested, packaged devices at its output.
- All assembled devices are subjected to an in-line surface-mount temperature profile pass to eliminate any remaining possibility, however small, of zero hour defects at the customer.
- Devices are packaged in industry standard blister pack reels for loading onto automatic pick-and-place machines.

5. SOT404

SOT404 (Figure 9, also known as TO263 and D^2PAK) possesses the same size of plastic body as SOT78 (TO220). The similarity ends there. SOT404 is manufactured without a tab since no mounting hole is required. (It is not merely a cropped TO220!) The center lead is cropped close to the plastic, so the "center leg connection" is made via the metal mounting base. The two outer leads are formed downwards to bring them into contact with the PCB.

5.1 SOT404 soldering

As for SOT428, it is also not possible to solder SOT404 using a wave soldering technique. The even larger body and larger hidden solder area would put this method out of the question. Reflow soldering is essential. Figure 8 shows typical SOT404 solder pad dimensions.

5.2 SOT404 design features for surface mounting

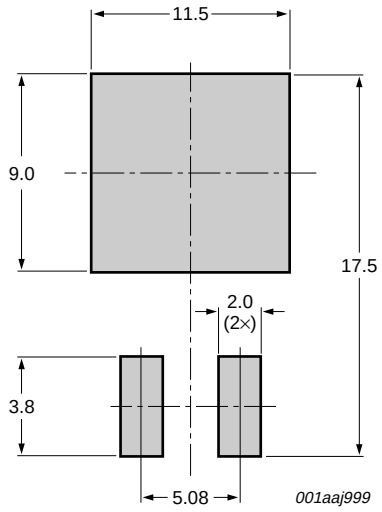
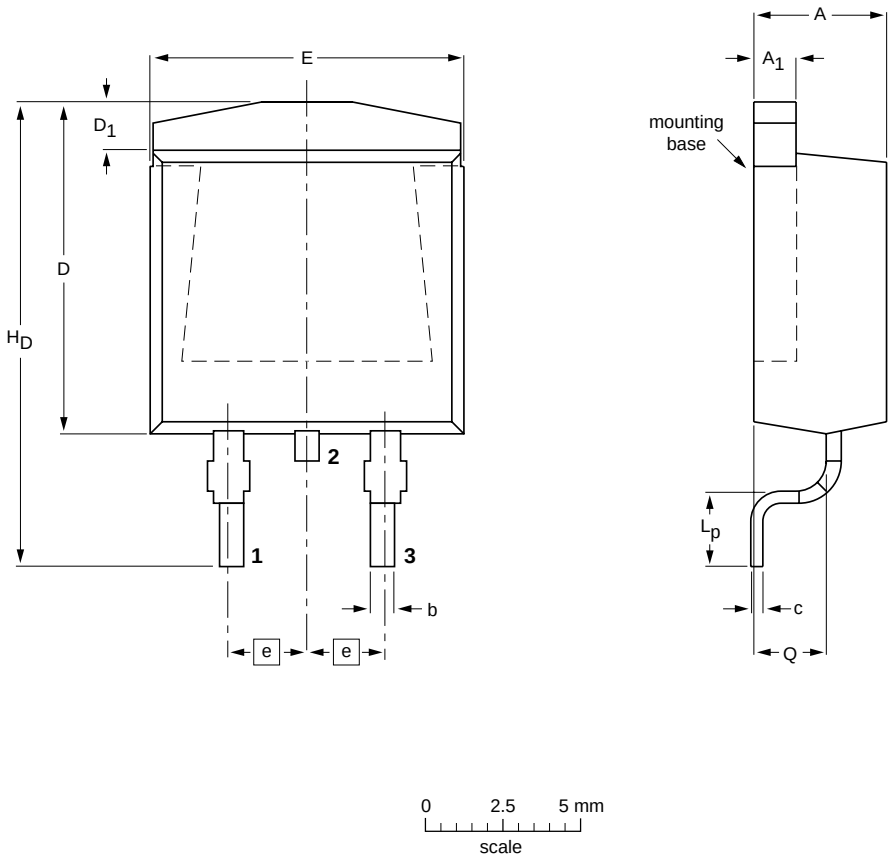


Fig 8. SOT404 solder pad

In designing and manufacturing the SOT404 package, similar measures must be taken as for SOT428 to ensure a reliable end product. These include:

- A low stress epoxy to minimize bending forces on the mounting base after curing (minimizes die stress).
- A thick copper mounting base of 1.4 mm (0.055 inch) max thickness to further minimize any tendency to bend.
- A low stress soft die bond solder (minimizes die stress).
- Accurate dosing and spreading of the die-attach solder prior to die bonding to ensure optimum die bonding over the complete die area every time without unsoldered areas or excess solder. This offers best long-term reliability under thermal cycling and optimum junction-to-mounting base thermal resistance.
- Optimized locking features to balance the conflicting requirements of good hermeticity with sufficient differential movement to avoid die stress fracture.
- A bare copper die pad to ensure good epoxy-to-metal adhesion for best hermeticity.
- Compatibility with the industry standard footprint layout for D^2PAK.
- Co-planarity check on leads to seating plane and leads to leads.
- A specially designed leadframe to reduce cropping forces as each device is separated from the comb. This avoids die cracking due to shock loading.
- A surface-mount temperature profile pass to eliminate zero hour defects at the customer.
- Devices are packaged in industry standard blister pack reels for loading onto automatic pick-and-place machines.

Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped) **SOT404**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	c	D max.	D_1	E	e	L_p	H_D	Q
mm	4.50 4.10	1.40 1.27	0.85 0.60	0.64 0.46	11	1.60 1.20	10.30 9.70	2.54	2.90 2.10	15.80 14.80	2.60 2.20

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT404						~~05-02-11~~ 06-03-16

Fig 9. Package outline SOT404

6. Mounting and soldering

The SM footprint drawings define the solder land (pad) areas, the solder resist areas and the area occupied by the package. Since the solder lands must be completely free of solder resist, the areas without the solder resist are always slightly greater than the solder land areas. The solder resist must cover all areas of the PCB that are not soldered to. This includes extended areas of copper used for heatsinking.

The footprints for reflow soldering define the solder paste areas in addition to the areas listed above. Solder paste is applied using a metal stencil which must be accurately aligned to within 0.1 mm over the pads. A metal "squeegee" is drawn across the stencil to deposit the paste through the apertures, which must be the same size as the solder paste areas defined on the footprint drawings. With reference to Figure 2 and Figure 3, it can be seen that the optimum pad areas are different for wave soldering and for reflow soldering.

When wave soldering, surface-mount devices must be held in position by a small measured dose of adhesive. A double wave process is used to ensure better wetting of all joints without solder shadows. Wave soldering **must** be used if there are any through-hole components on the PCB.

During reflow soldering, surface-mount devices are held in position by the viscosity of the solder paste. When the solder is melted in the reflow oven, the surface tension of the molten solder causes them to self-center on their pads. The pad sizes and configuration are critical if self-centring is to operate reliably.

Both soldering methods are sometimes employed on PCBs containing a mixture of surface-mount and through-hole components, in order to ensure optimum soldering of both technologies.

A more detailed description of the wave and reflow soldering processes is beyond the scope of this Technical Publication.

7. Thermal resistance: a laboratory investigation

Detailed laboratory tests have been conducted on the junction-to-ambient thermal resistance $R_{th(j-a)}$ of the SOT223, SOT428 and SOT404 SM packages when mounted to different pad sizes on standard FR4 PCB. Sufficient time was devoted to this work to ensure repeatability of the results and to give a high level of confidence in their validity.

7.1 Theory

It is possible to measure the temperature of a power semiconductor junction by measuring one of its temperature-dependent characteristics. With a MOSFET for example, it might be the forward voltage of the anti-parallel diode and for a thyristor it would be the on-state voltage (V_T). In order to heat up the device under test, a heating current is passed through it. When measuring its temperature-dependent characteristic, a much lower calibration current is passed for a very short measurement period.

SCRs were used for this investigation because of the relative ease of measurement. (SCRs only have to be measured in one direction, whereas triacs have to be measured in forward and reverse directions and the results combined.)

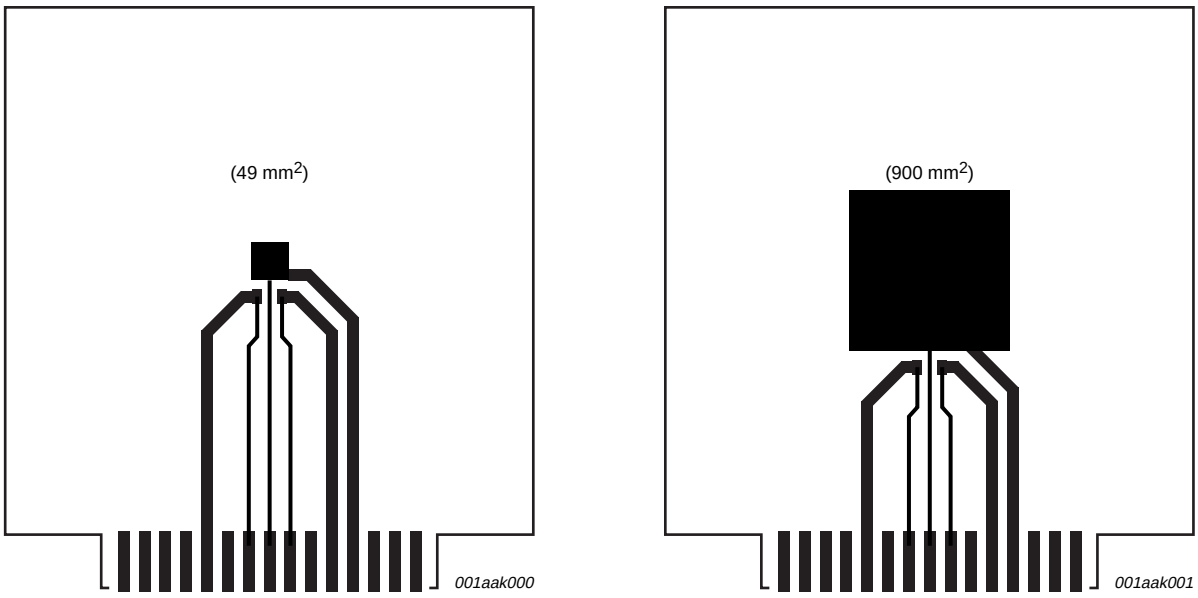
The size of the die within any given package will not affect the final $R_{th(j-a)}$ result appreciably because any differences in the junction-to-case thermal resistance $R_{th(j-c)}$ will be insignificant compared to the case-to-ambient thermal resistance $R_{th(c-a)}$. It is not critical, therefore, which device is used when measuring package R_{th} in free air or when surface mounted to conventional PCBs with relatively high thermal resistances to ambient.

FR4 fiberglass PCB with 35 µm copper (1 oz/square foot) was used because it is an industry standard to which everyone can relate. It is the PCB type that is always quoted in power semiconductor manufacturers' data sheets. It has become a "reference standard" by default. Despite this "standard" status, many industries cannot justify its use because of its cost. The home appliance industry prefers to use a lower cost alternative, one example of which is CEM3. This is a resin and paper-based material with fiber on both sides. Fortunately, the thermal performance of the cheaper alternatives is sufficiently close to that of FR4 in many cases to make the results of this investigation valid for those also.

7.2 Equipment

The test PCBs had pad sizes that varied upwards from the minimum recommended for the package. Consistent pad width : height ratios were maintained. The pad was always positioned centrally on the test board to assure consistent heatsinking to the bulk of the PCB. SOT223 and SOT428 used the same pad layouts, while SOT404 had its own PCBs. Figure 10 shows the second smallest and largest pad size test boards for SOT223/ SOT428, and Figure 11 shows the smallest and largest pad size test boards for SOT404.

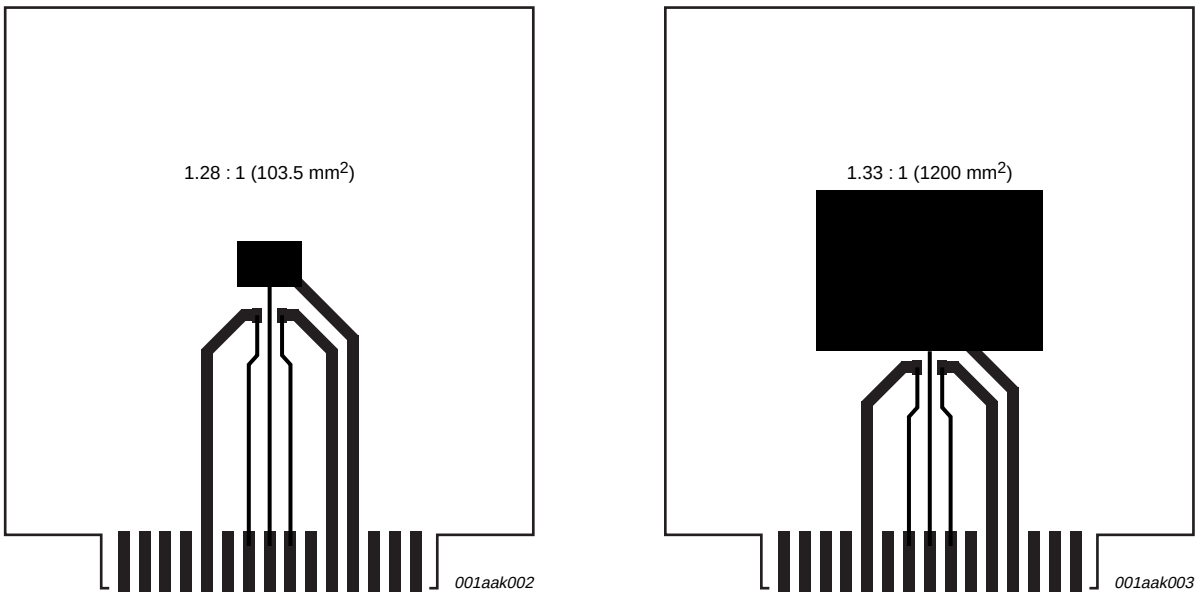
Remark: The following test boards are not shown at 1 : 1 scale.



a. Small pad area

b. Large pad area

Fig 10. SOT223 and SOT428 test PCB layout



a. Small pad area

b. Large pad area

Fig 11. SOT404 test PCB layout

Separate power and measurement connections were taken via an edge connector to the device. The PCBs were standard fiberglass FR4 with 35 µm copper, which had been very lightly "tinned" by electrochemical deposition. (Thermal resistance will not be reduced by a thick layer of roller tinning.) The PCBs were made relatively large at 100 mm × 100 mm to ensure that R_{th} is controlled by pad area and not by PCB area.

SCRs were tested using a purpose built thermal resistance test gear. (SCRs were tested in preference to triacs because they only require one measurement for each power setting, whereas triacs need measuring in both directions with the average power being calculated from the results.)

The most important fact to remember when conducting the tests was that they take a lot of time. It was essential to ensure that thermal equilibrium and stability had been reached before readings were taken at elevated device temperature. Rushing the tests would give incorrect results and improbable graphs. This was learned from experience.

7.3 Results

The resolution and accuracy of the final $R_{th(j-a)}$ results were maximized by generating high values of ΔT_j, hence large measured voltage variations (ΔV). The results tables show $R_{th(j-a)}$ (K/W) versus power dissipation and pad area. The power levels highlighted with table notes indicate a suggested power dissipation limit for the package when soldered to the minimum pad area on FR4 PCB. (In the case of the SOT223 package, the smallest pad area used was 20 mm^2. This area is fully occupied by the SOT428 package. The minimum for SOT223 is actually 5.7 mm^2. Therefore the 1 W power dissipation achieved in these experiments will be higher than that achievable with a 5.7 mm^2 pad. 0.5 W is likely to be the practical maximum power dissipation for SOT223 on a 5.7 mm^2 pad.)

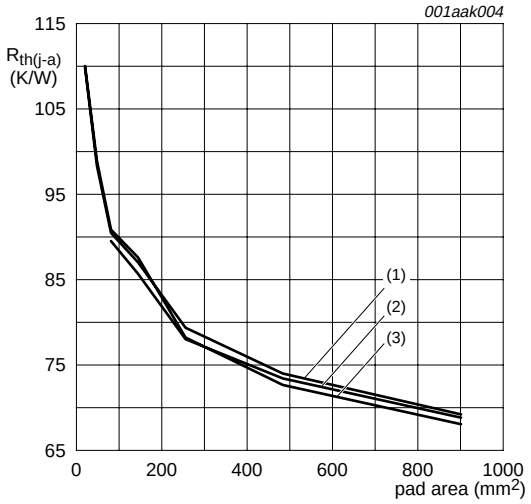
The results graphs show $R_{th(j-a)}$ versus pad area and ΔT_j versus pad area. With any given package, higher power dissipation leads to higher ΔT_j, which in turn leads to lower $R_{th(j-a)}$. This is because a larger temperature difference results in more efficient radiation to ambient.

Table 1. SOT223 thermal characteristics

SOT223 $R_{th(j-a)}$ against pad area and power dissipation.

Area (mm^2)	0.5 W	1.0 W[1]	1.5 W
20	110	110	-
49	99	98	-
81	91	90	90
144	88	87	86
256	78	79	78
484	73	74	73
900	68	69	69

[1] The suggested power dissipation limit for the package when soldered to the minimum pad area on FR4 PCB.



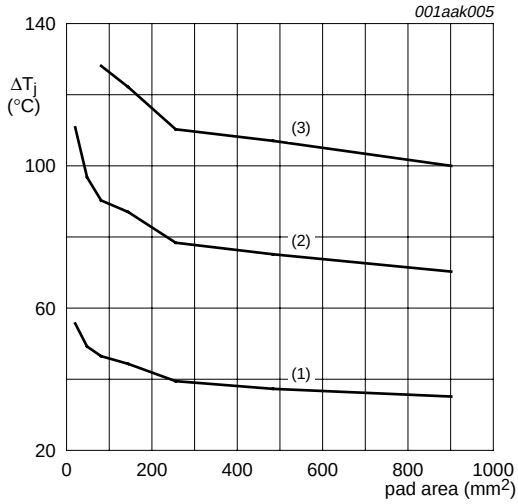
100 × 100 mm FR4 PCB positioned vertically in still air.

(1) 0.5 W

(2) 1.0 W

(3) 1.5 W

Fig 12. SOT223 $R_{th(j-a)}$ against PCB pad area



100 × 100 mm FR4 PCB positioned vertically in still air.

(1) 0.5 W

(2) 1.0 W

(3) 1.5 W

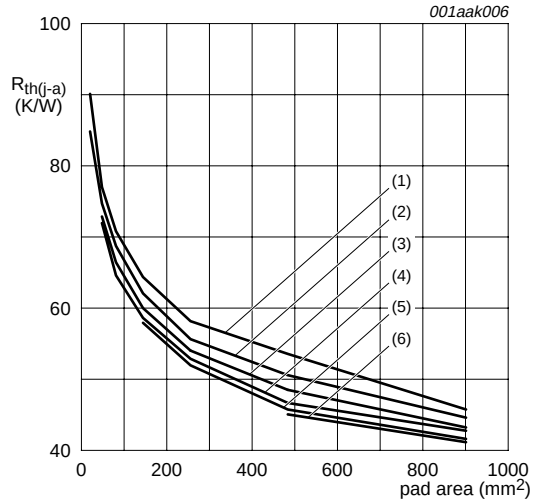
Fig 13. SOT223 junction temperature rise against PCB pad area

Table 2. SOT428 thermal characteristics

SOT428 $R_{th(j-a)}$ against pad area and power dissipation

Area (mm^2)	0.5 W	1.0 W[1]	1.5 W[1]	2.0 W	2.5 W	3.0 W
20	90	85	-	-	-	-
49	77	75	73	72	-	-
81	71	69	66	65	-	-
144	64	62	60	59	58	-
256	58	56	54	53	52	-
484	54	50	48	47	46	45
900	46	45	43	43	42	41

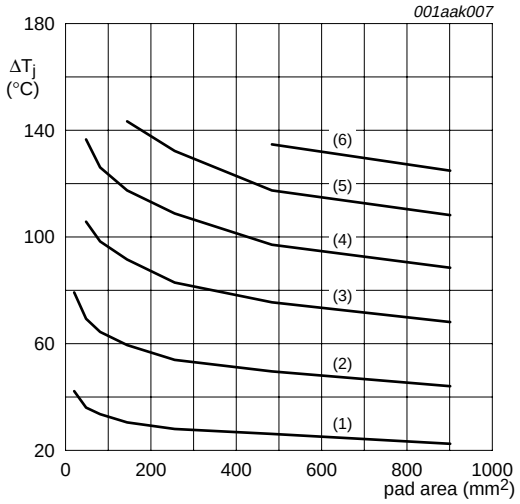
[1] The suggested power dissipation limit for the package when soldered to the minimum pad area on FR4 PCB.



100 × 100 mm FR4 PCB positioned vertically in still air.

(1) 0.5 W
(2) 1.0 W
(3) 1.5 W
(4) 2.0 W
(5) 2.5 W
(6) 3.0 W

Fig 14. SOT428 $R_{th(j-a)}$ against PCB pad area



100 × 100 mm FR4 PCB positioned vertically in still air.

(1) 0.5 W
(2) 1.0 W
(3) 1.5 W
(4) 2.0 W
(5) 2.5 W
(6) 3.0 W

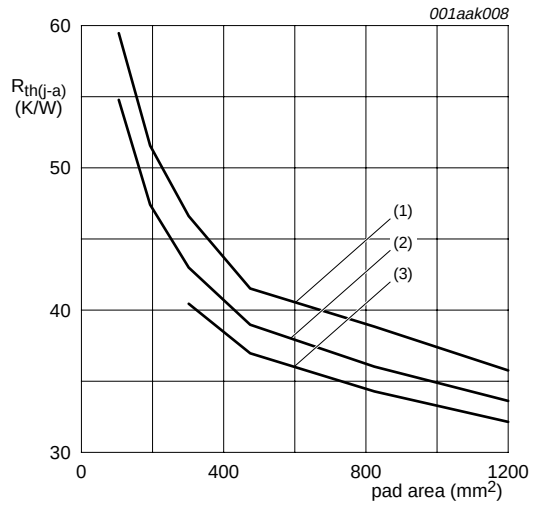
Fig 15. SOT428 junction temperature rise against PCB pad area

Table 3. SOT404 thermal characteristics

SOT404 $R_{th(j-a)}$ against pad area and power dissipation

Area (mm^2)	1.0 W	2.0 W[1]	3.0 W
103.5	60	55	-
192	52	47	-
300	47	43	41
475	41	39	37
825	39	36	34
1200	36	34	32

[1] The suggested power dissipation limit for the package when soldered to the minimum pad area on FR4 PCB.



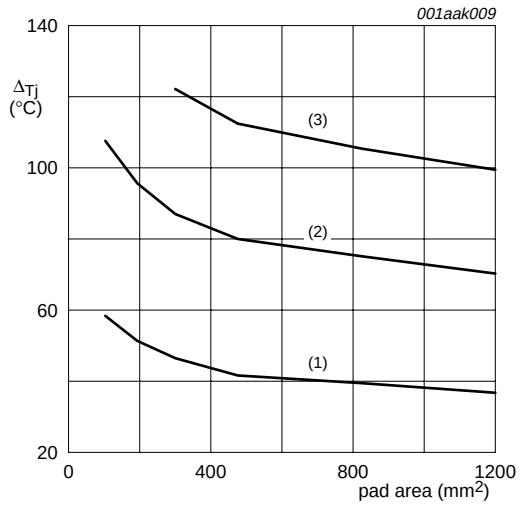
100 × 100 mm FR4 PCB positioned vertically in still air.

(1) 1.0 W

(2) 2.0 W

(3) 3.0 W

Fig 16. SOT404 $R_{th(j-a)}$ against PCB pad area



100 × 100 mm FR4 PCB positioned vertically in still air.

(1) 1.0 W

(2) 2.0 W

(3) 3.0 W

Fig 17. SOT404 junction temperature rise against PCB pad area

8. Conclusion

The maximum practical power dissipations are summarized below for stagnant ambient conditions at 25 °C. These are for standard FR4 PCB or similar without special heatsinking provisions. The 35 μm copper had been lightly tinned by electrochemical deposition.

SOT223 and SOT428 can be soldered to common pad layouts. 20 mm^2 was the absolute minimum pad area for soldering SOT428. The reasonable power dissipation for SOT428 on 20 mm^2 fell somewhere between 1.0 W and 1.5 W.

The minimum pad quoted in data for SOT223 is 5.7 mm^2. 0.5 W is the more realistic maximum power dissipation for SOT223 on its minimum pad.

Table 4. Overview of package characteristics

Package	P_{max} (W)	Pad area (mm^2)	ΔT_j (°C)	$R_{th(j-a)}$ (K/W)	
				Experimental	Specified in data
SOT223	1.0	20	97	99	156 (5.7 mm^2 pad)
		650	74	72	70 (648 mm^2 pad)
SOT428	1.0 < 1.5	20	106	73	75
SOT404	2.0	104	108	55	55

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10. Figures

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Date of release: 21 April 2009
Document identifier: AN10805_1